

FIG. 1A

00055851.051601

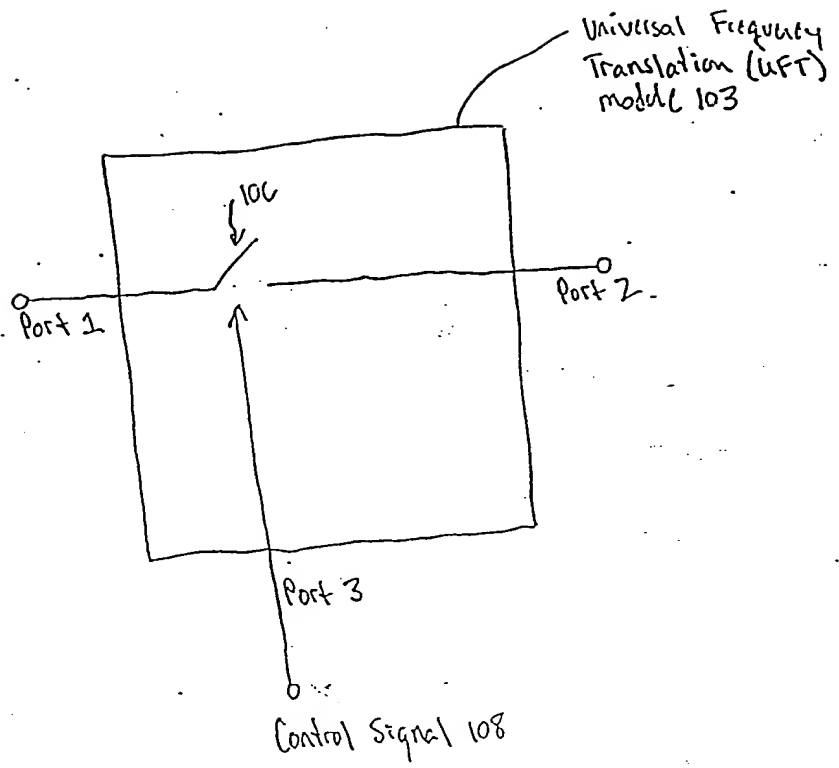


FIG. 1B

09855851.051601

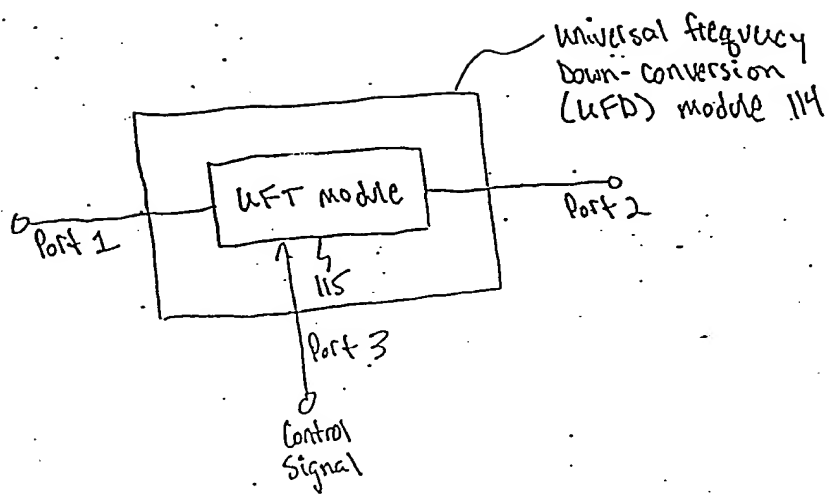


FIG. 1C

09655854.051604

09855851.051601

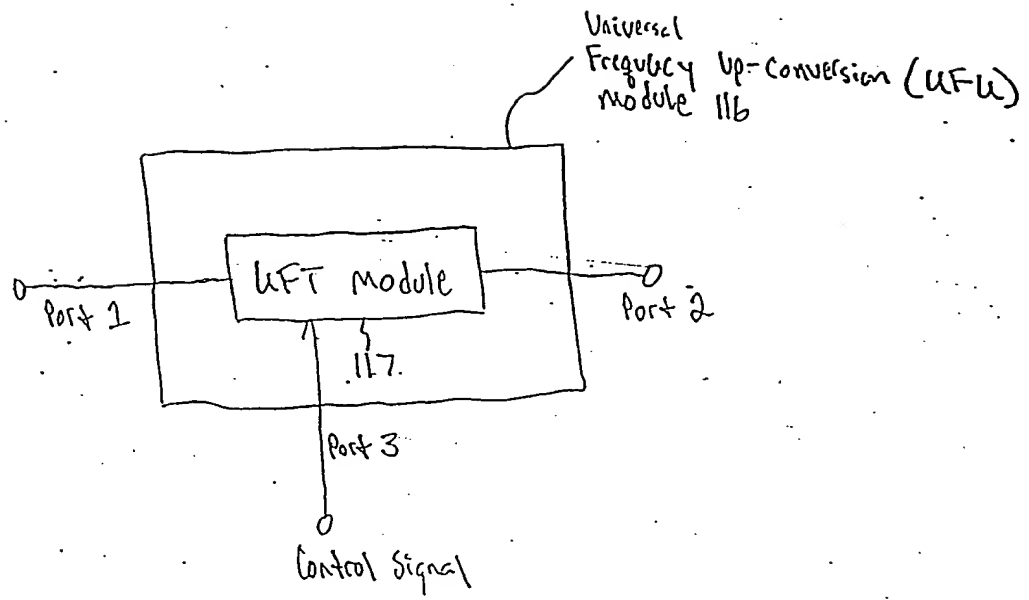


FIG. 1D

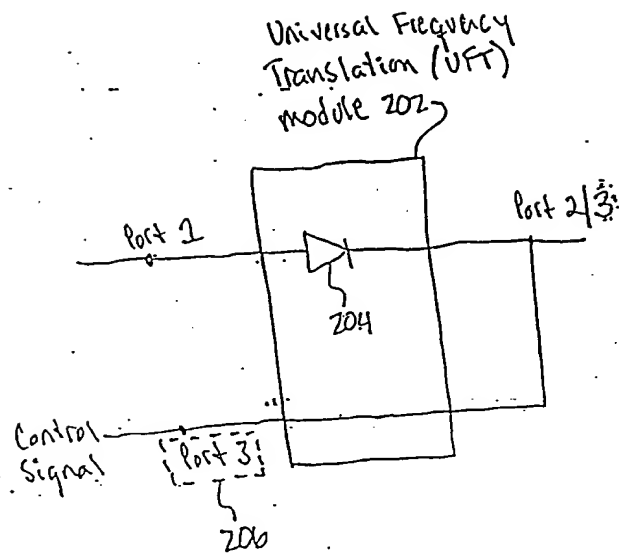


FIG. 2

3

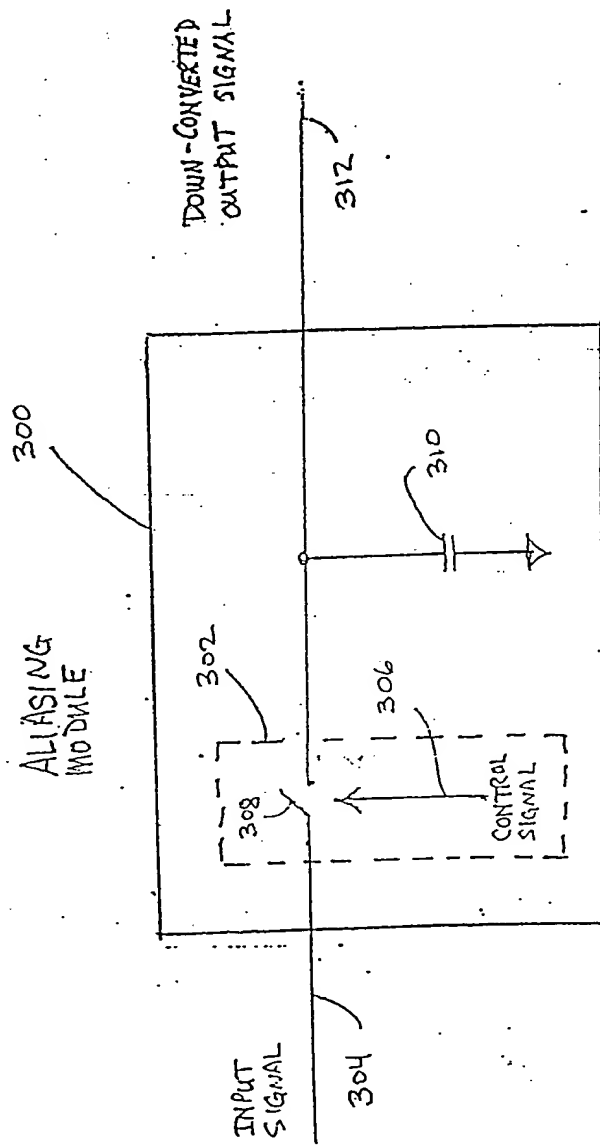


FIG. 3A

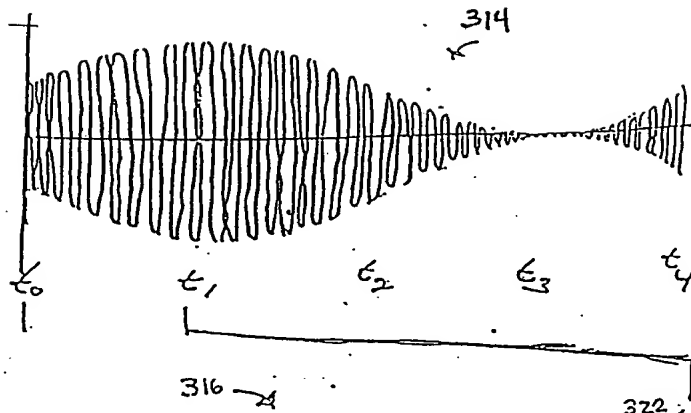


FIG. 3B

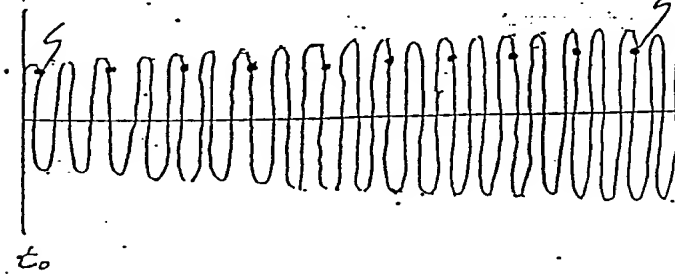


FIG. 3C

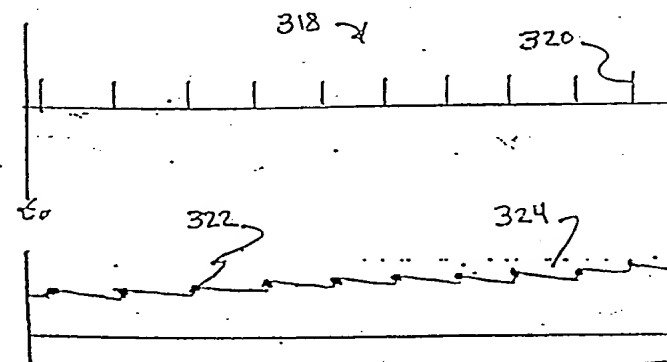


FIG. 3D

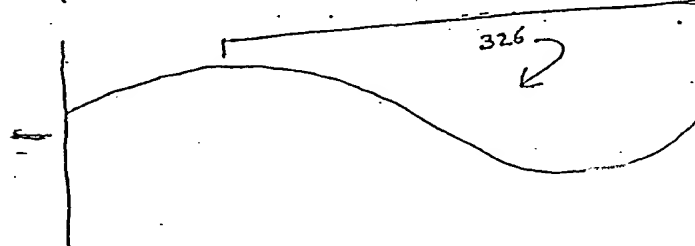


FIG. 3E

FIG. 3F

09855851.051601

# ALIASING MODULE

300

DOWN-CONVERTED  
OUTPUT SIGNAL

312

INPUT  
SIGNAL

304

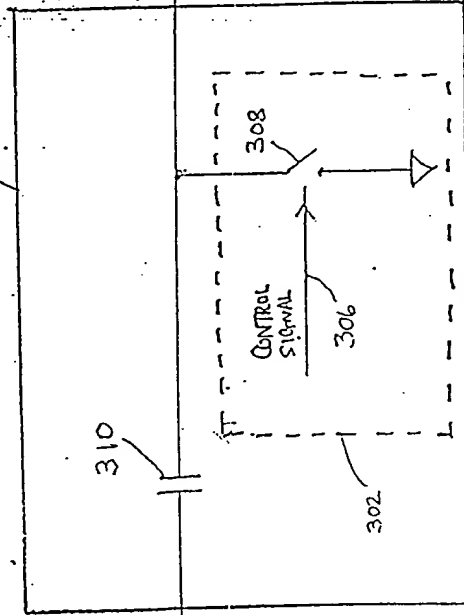


FIG. 3G



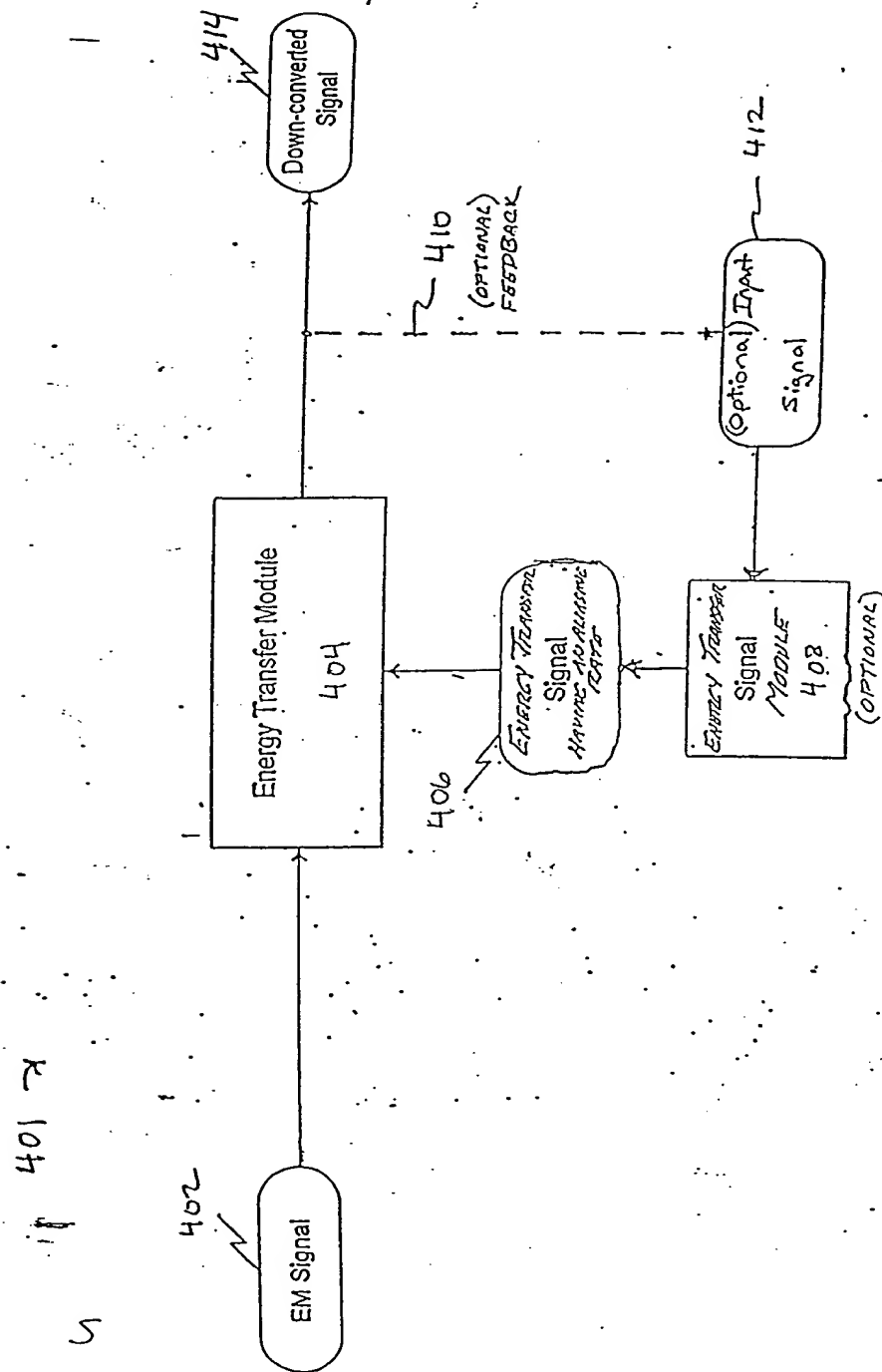


FIG. 4

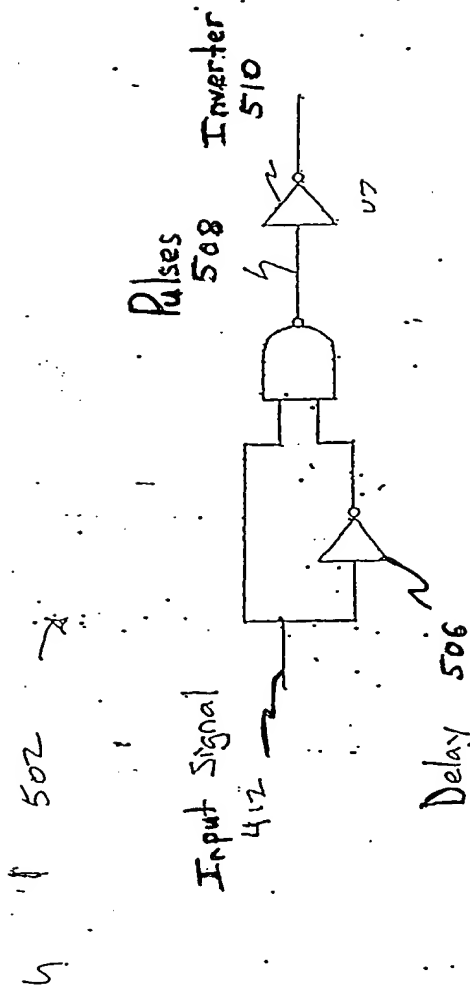


FIG. 5

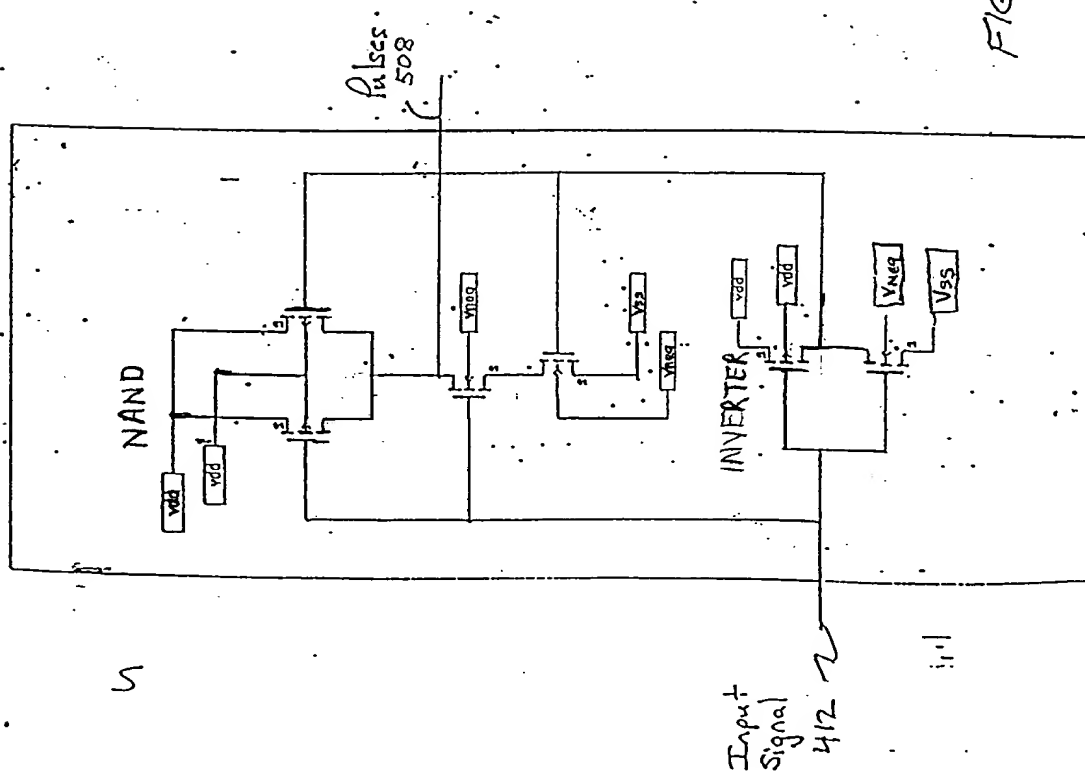


FIG. 6A

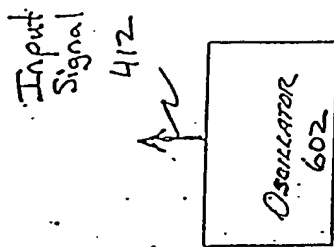


FIG. 6B

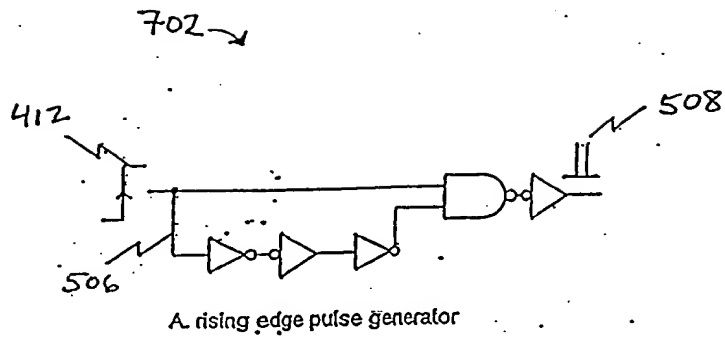


FIG. 7A

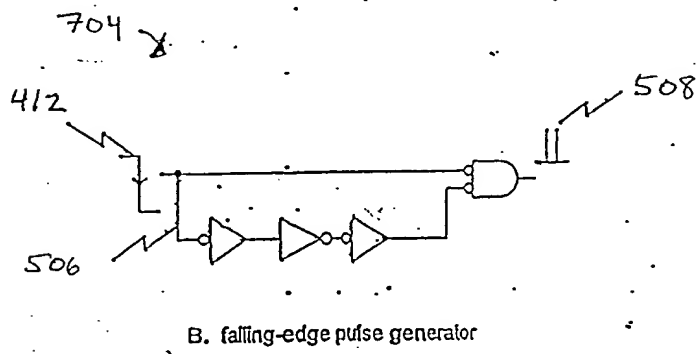


FIG. 7B

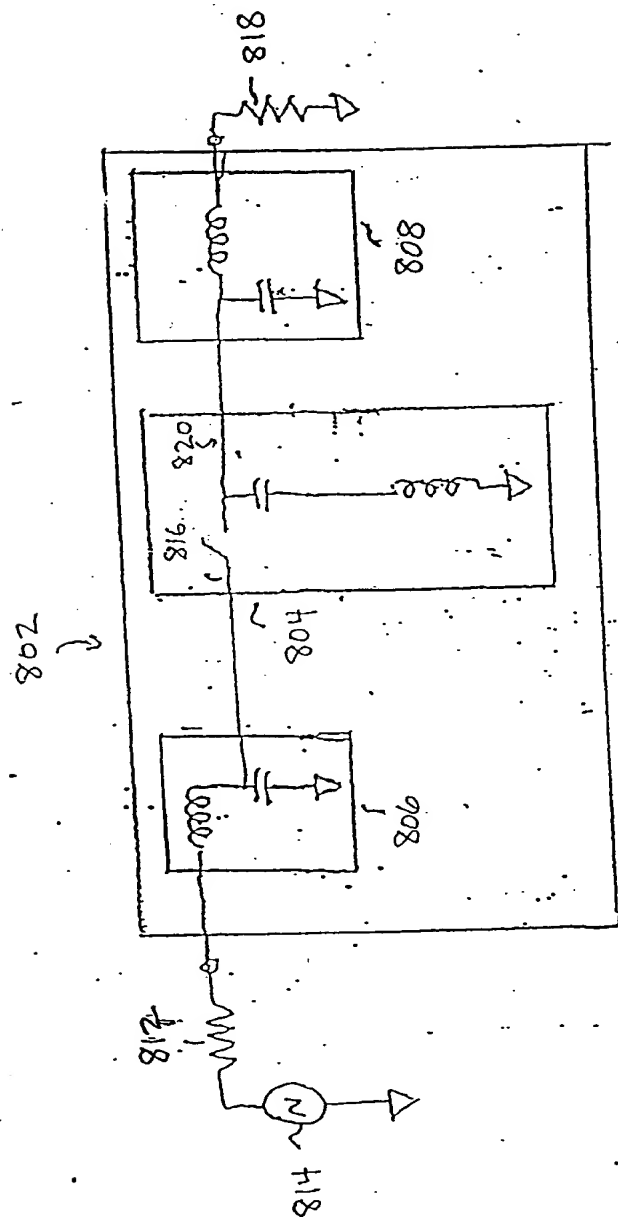


Fig. 8 - Impedance Matched Aliasing Module

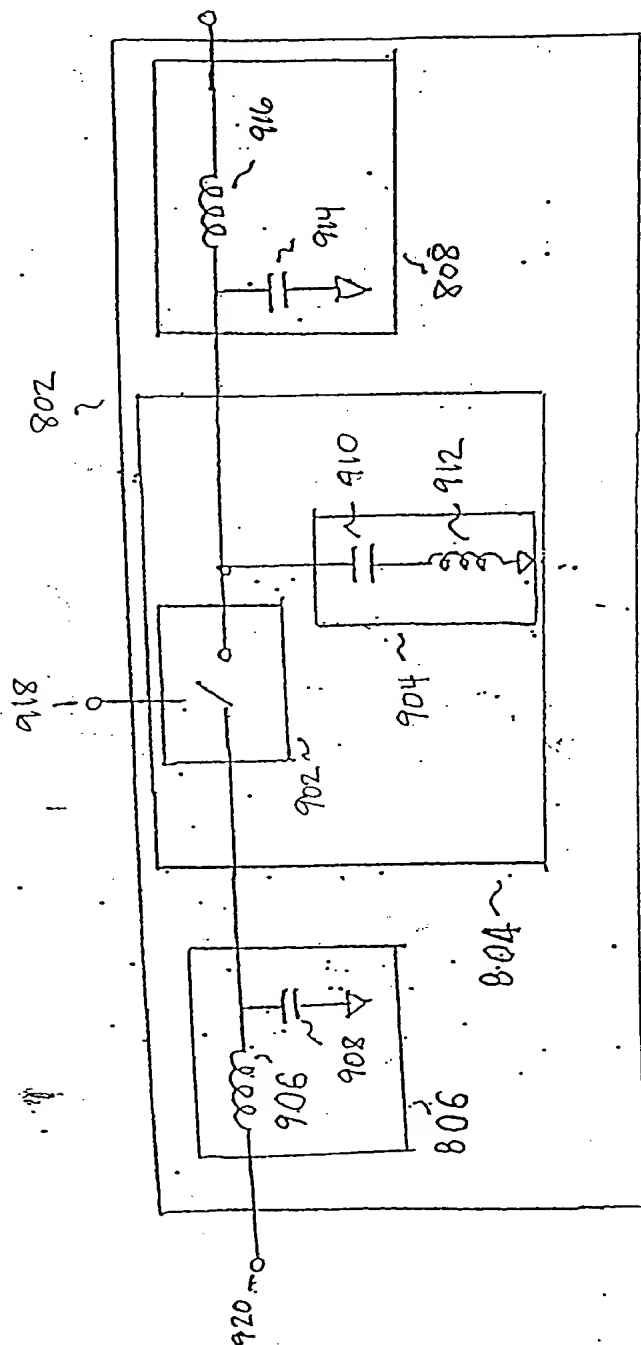


Fig 9 - Aliasing Module

Universal Frequency  
Up-Conversion (UFU) module 1000

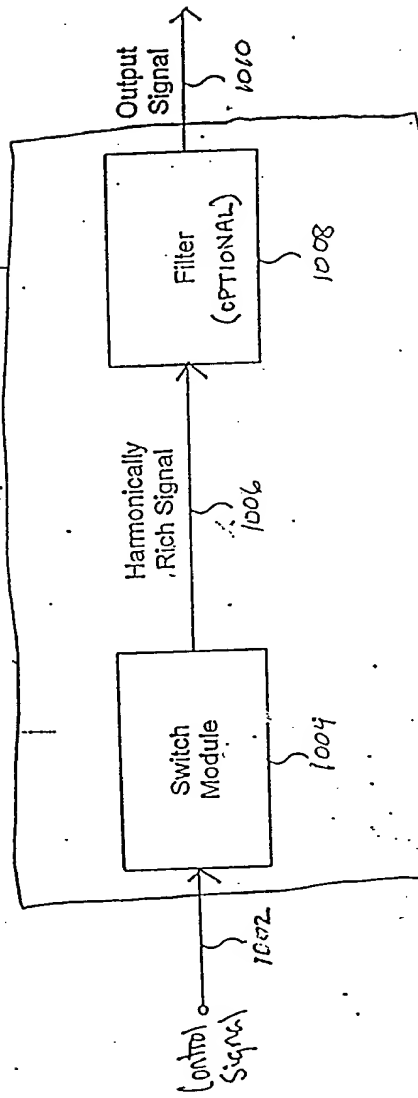


FIG. 10

Universal Frequency  
Up-Conversion (UFC) module 1101

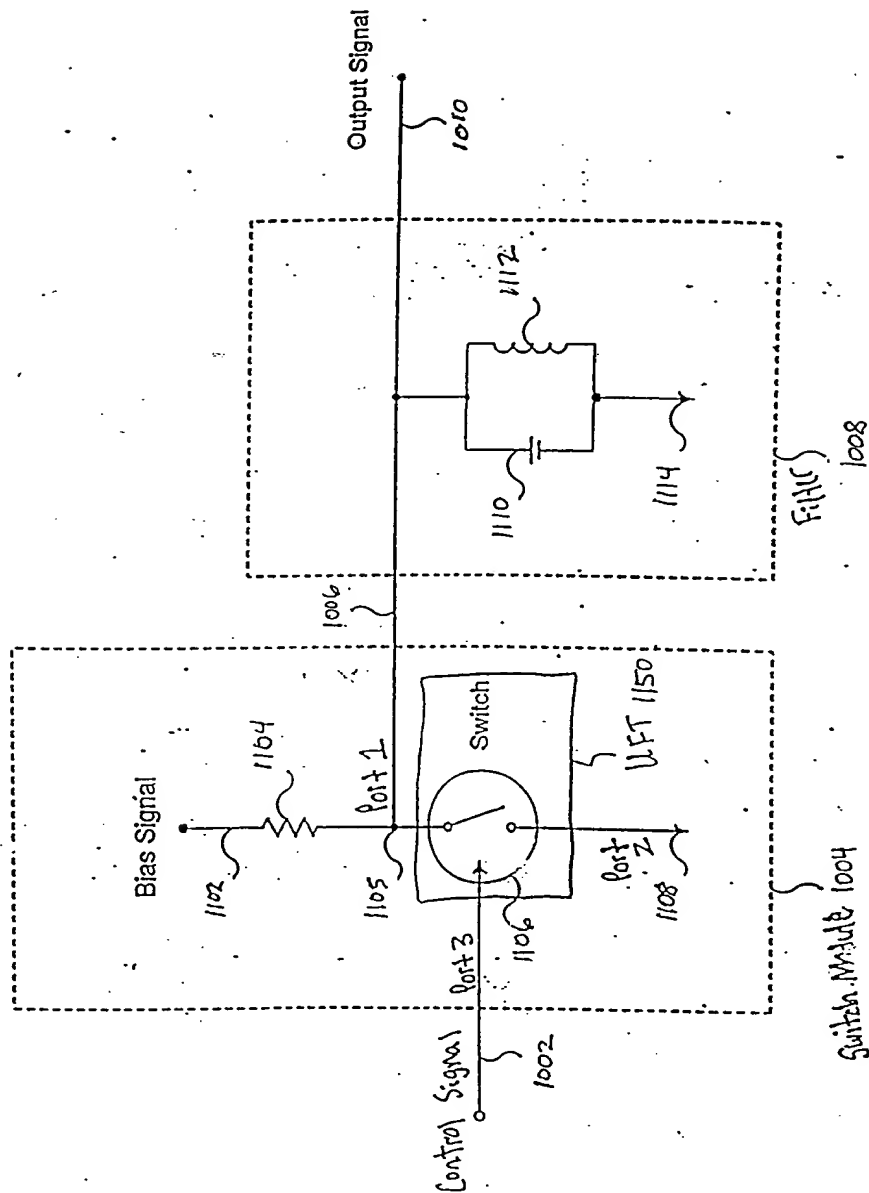


FIG. 11



Universal Frequency  
Up-Conversion  
(UFU) module 1290

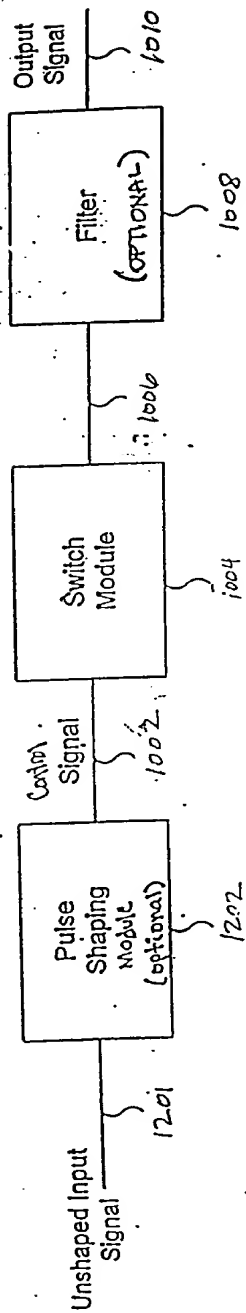


FIG. 12

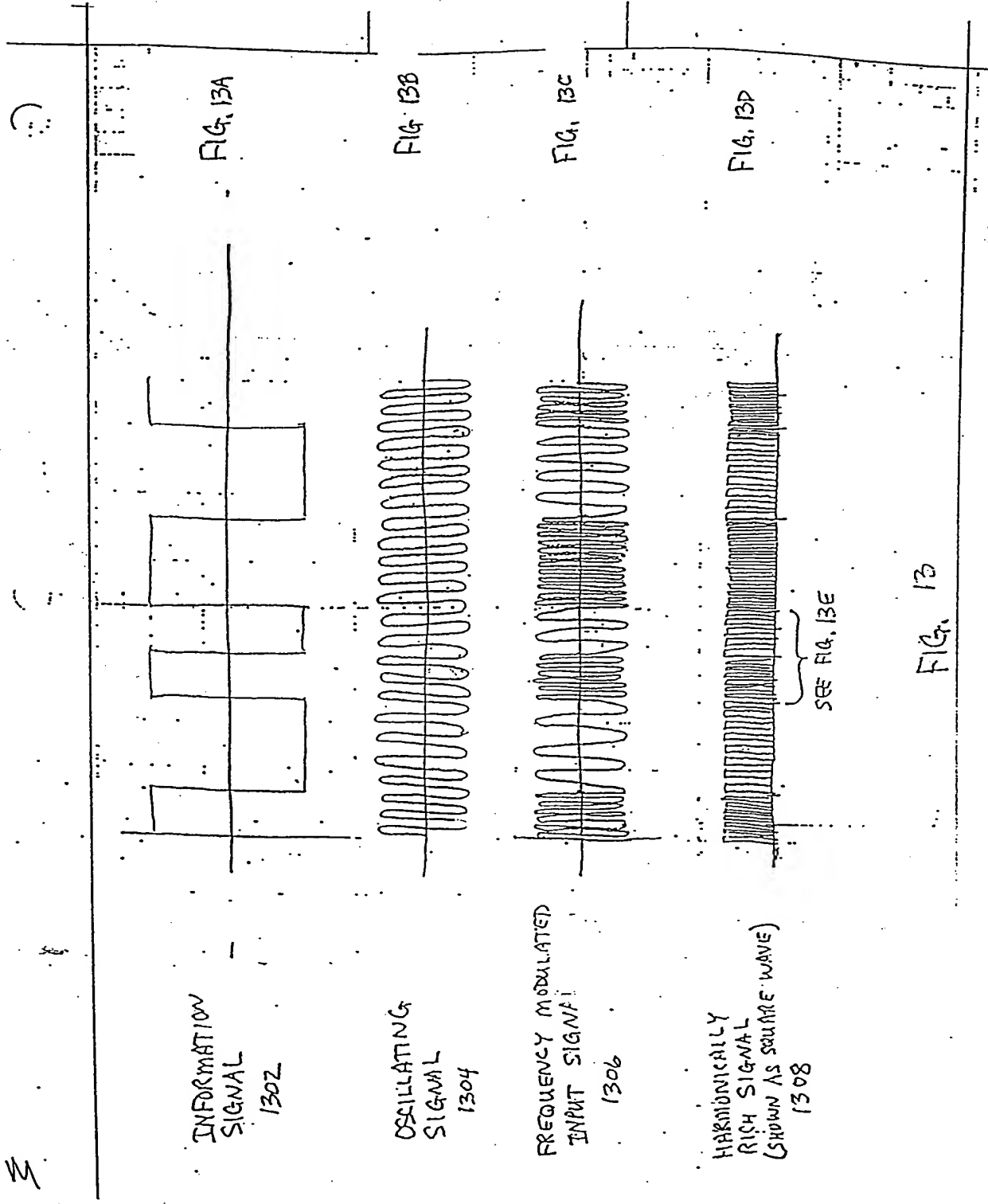


FIG. 13

EXPANDED VIEW OF  
HARMONICALLY RICH  
SIGNAL 1308

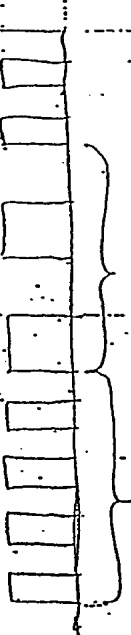


FIG 13E

HARMONICS OF  
SIGNAL 1310  
(SHOWN SEPARATELY)

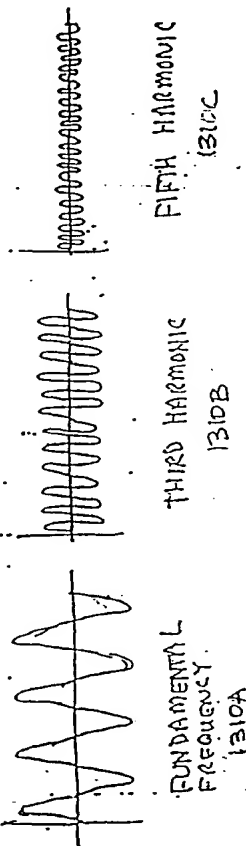


FIG 13F

HARMONICS OF  
SIGNAL 1312  
(SHOWN SEPARATELY)

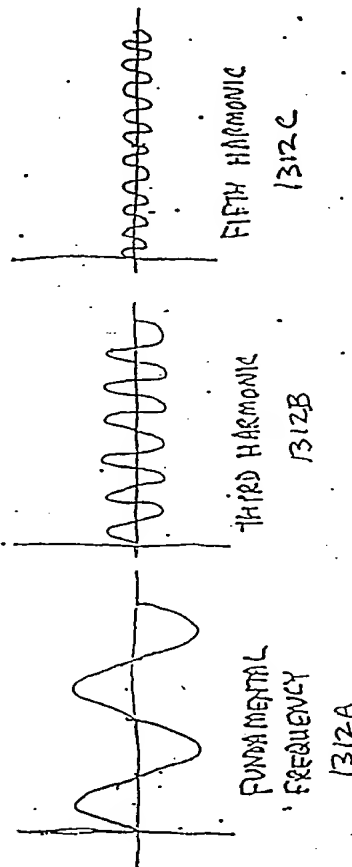


FIG 13G

FIG. 13 (cont)

HARMONICS OF  
SIGNALS 1310 AND  
1312. (SHOWN  
SIMULTANEOUSLY BUT  
NOT SUMMED)

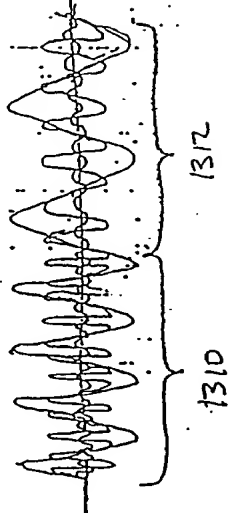


FIG 13H

ALTERED  
OUTPUT  
SIGNAL  
1314

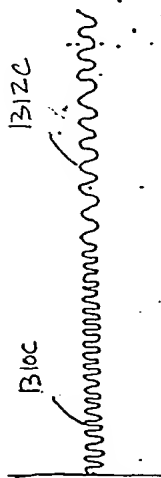


FIG. 13I

FIG 13 (cont)

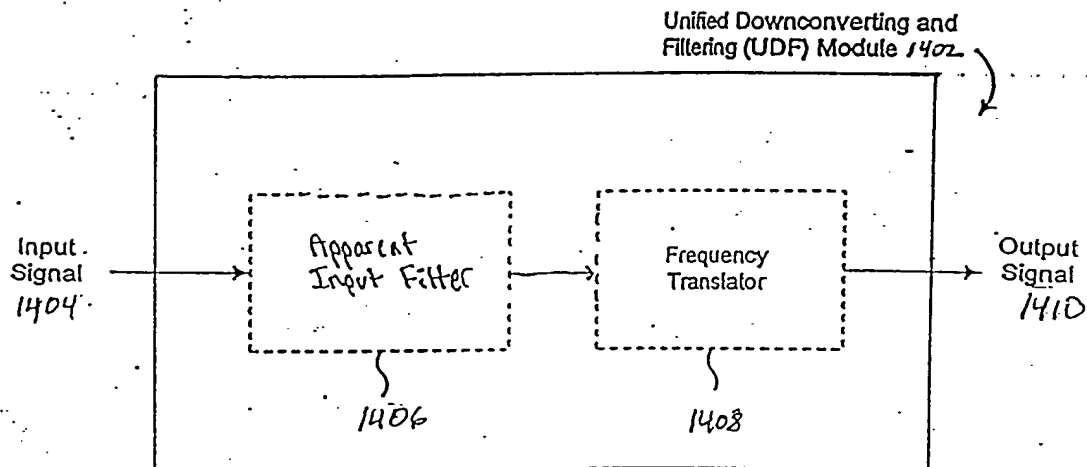


FIG. 14

m

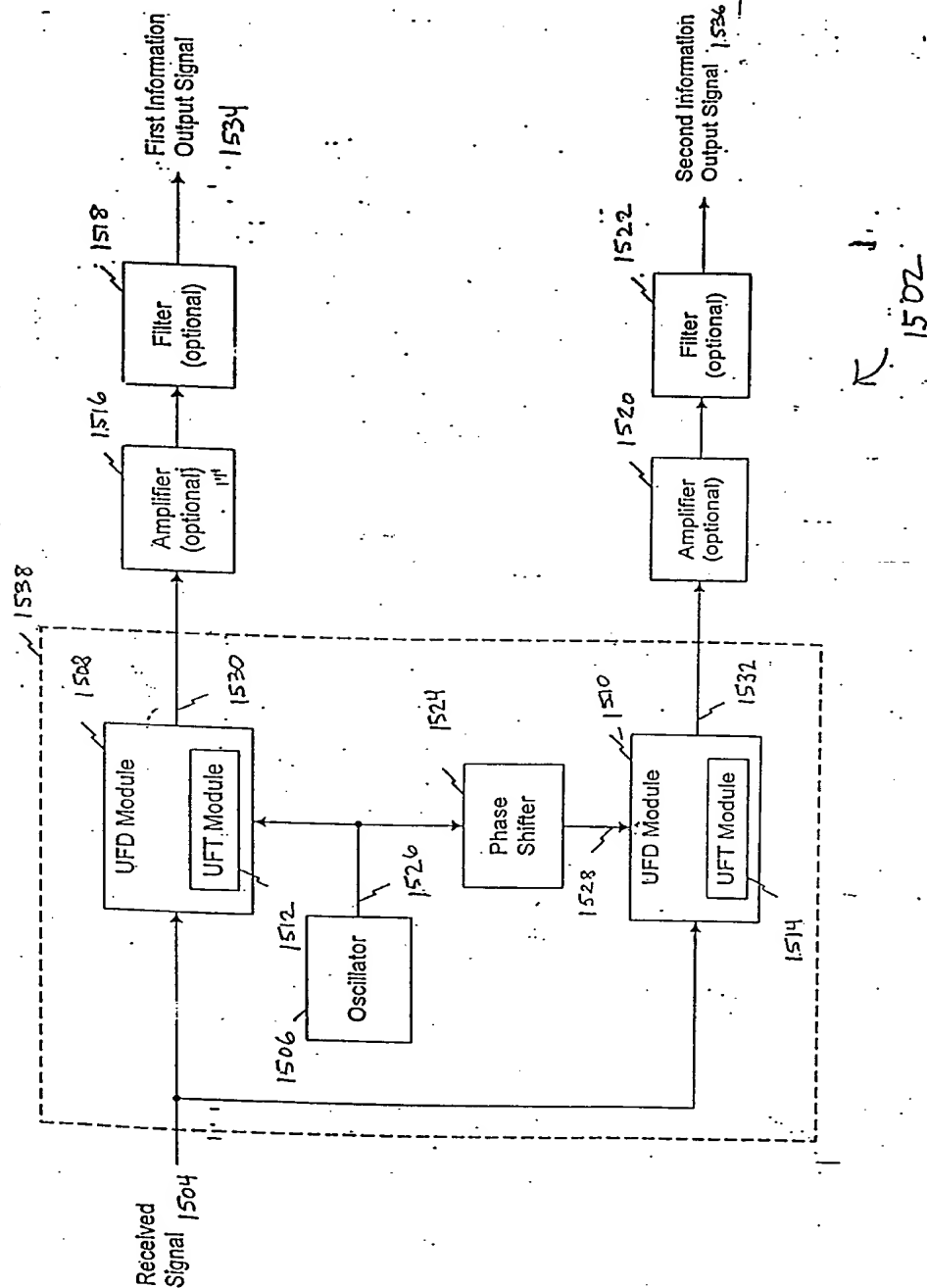


FIG. 15

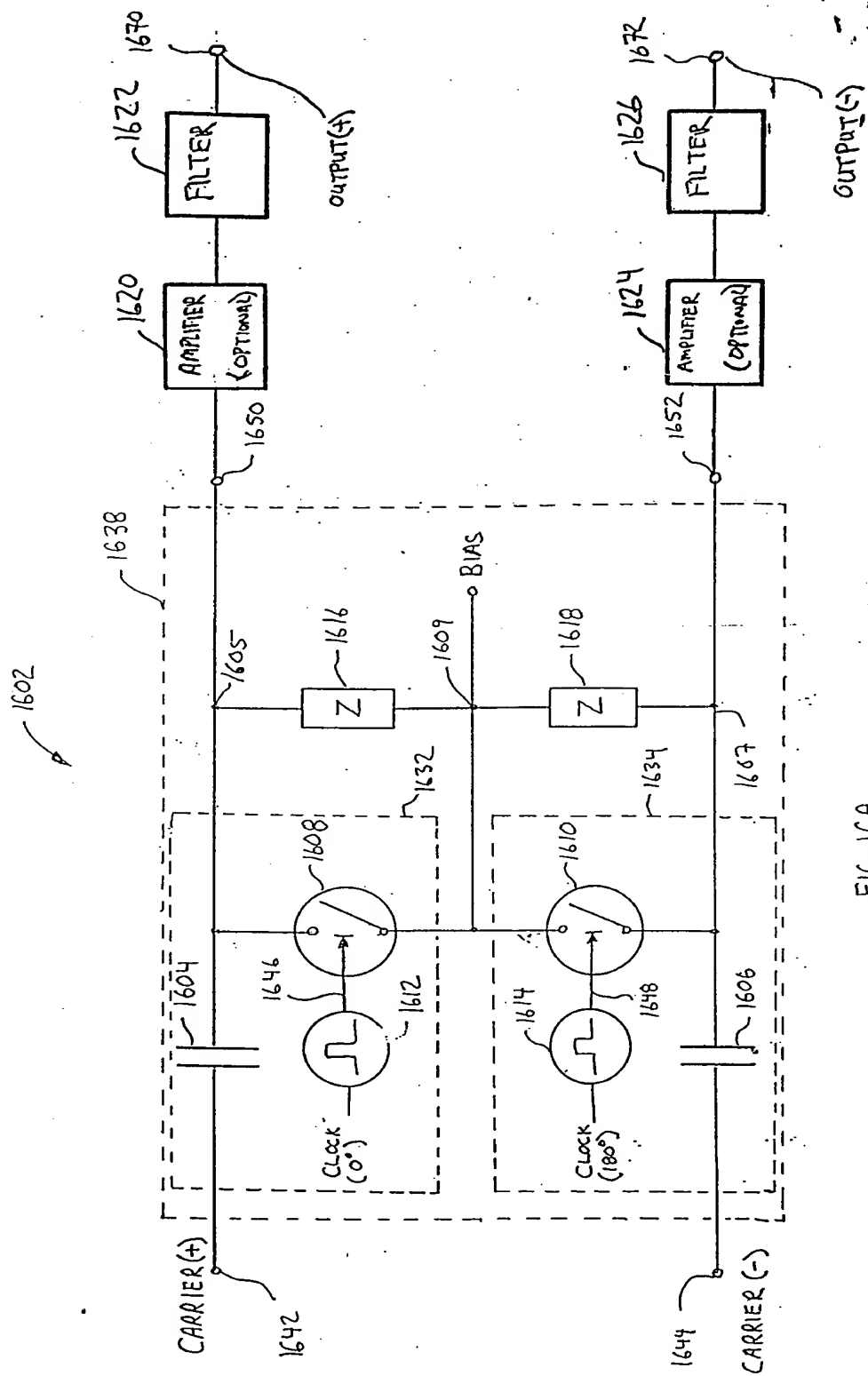


FIG. 16A

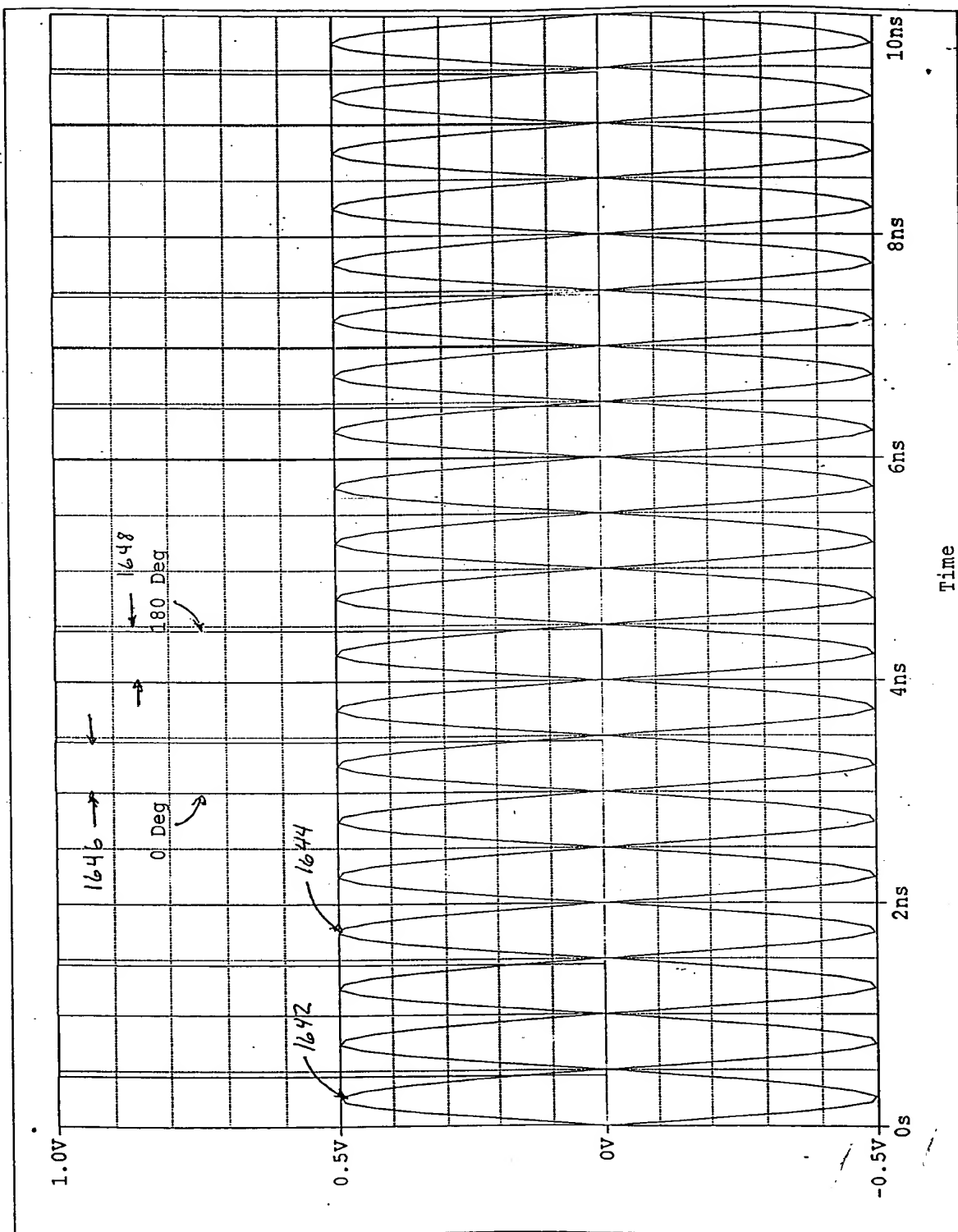


FIG. 16 B



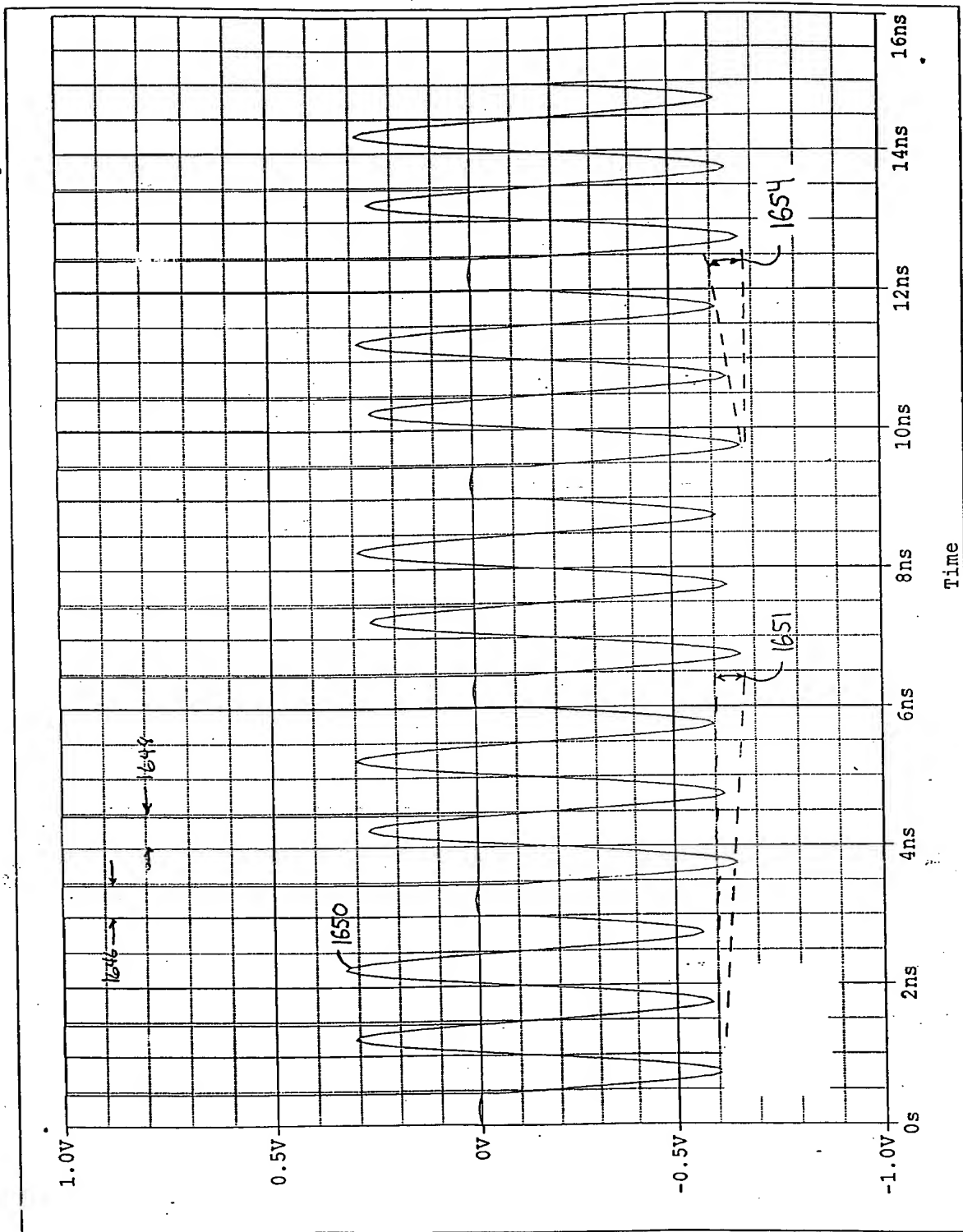


FIG. 16C

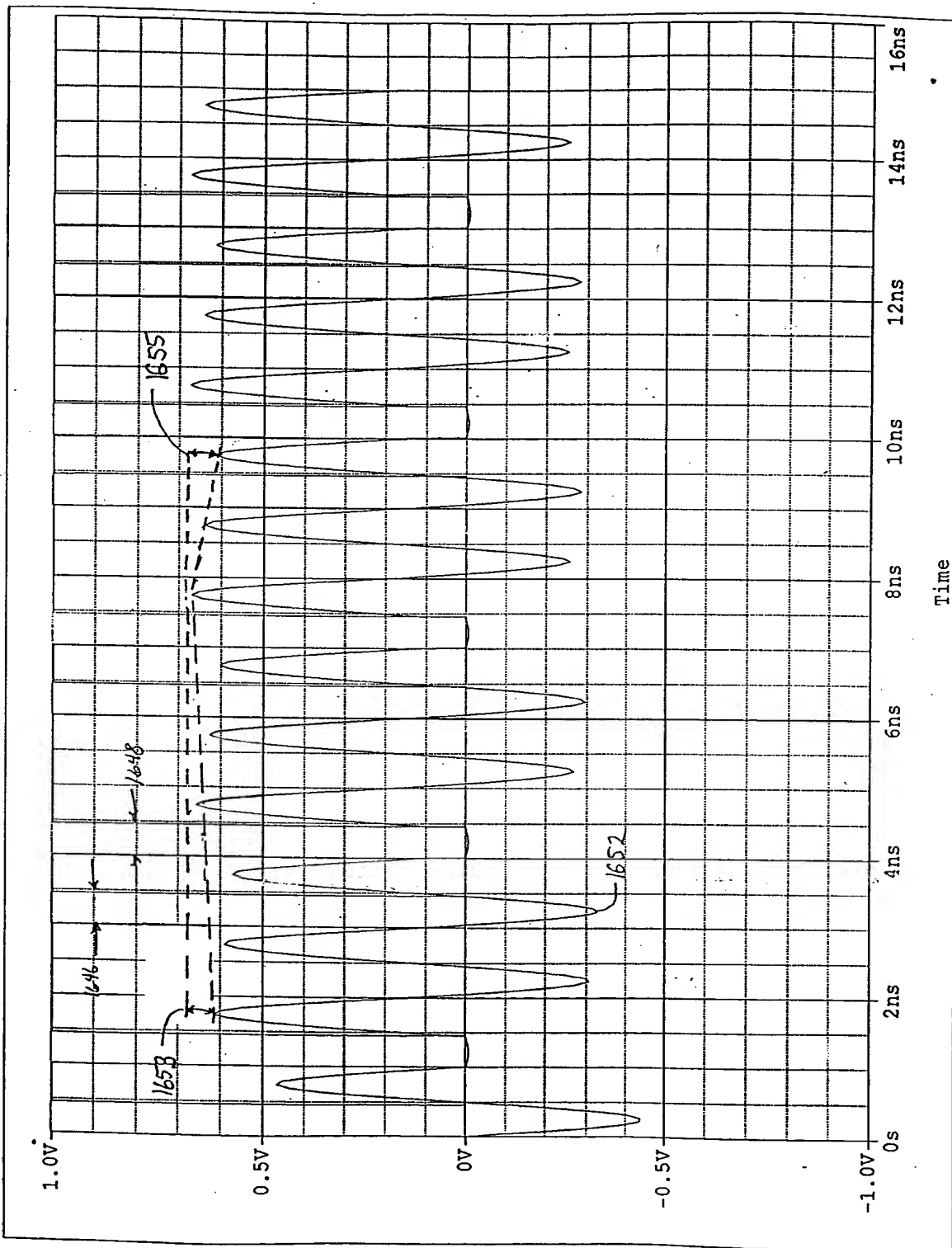


FIG. 16D

FOOTNOTES

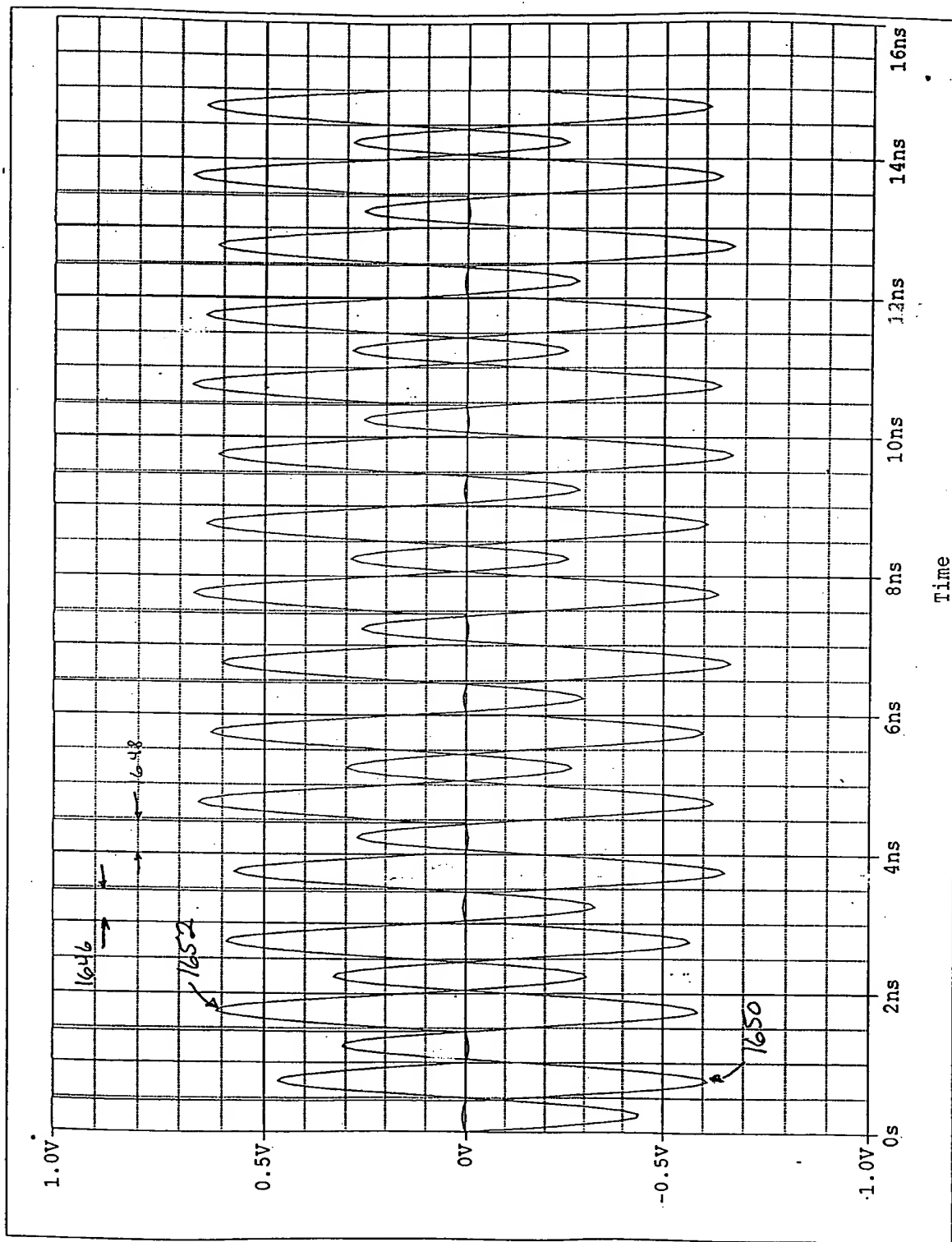


FIG. 16E

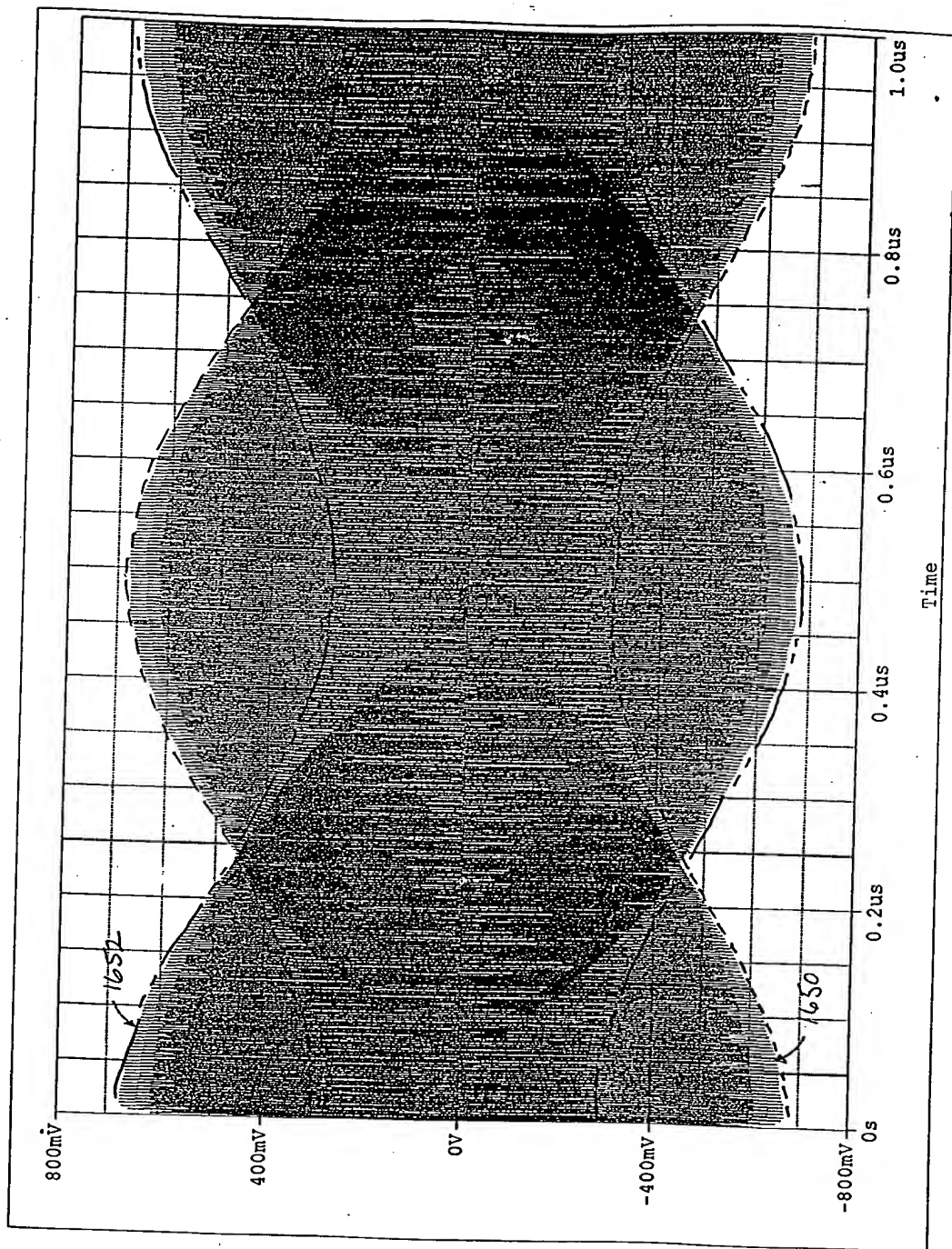


FIG. 16 F

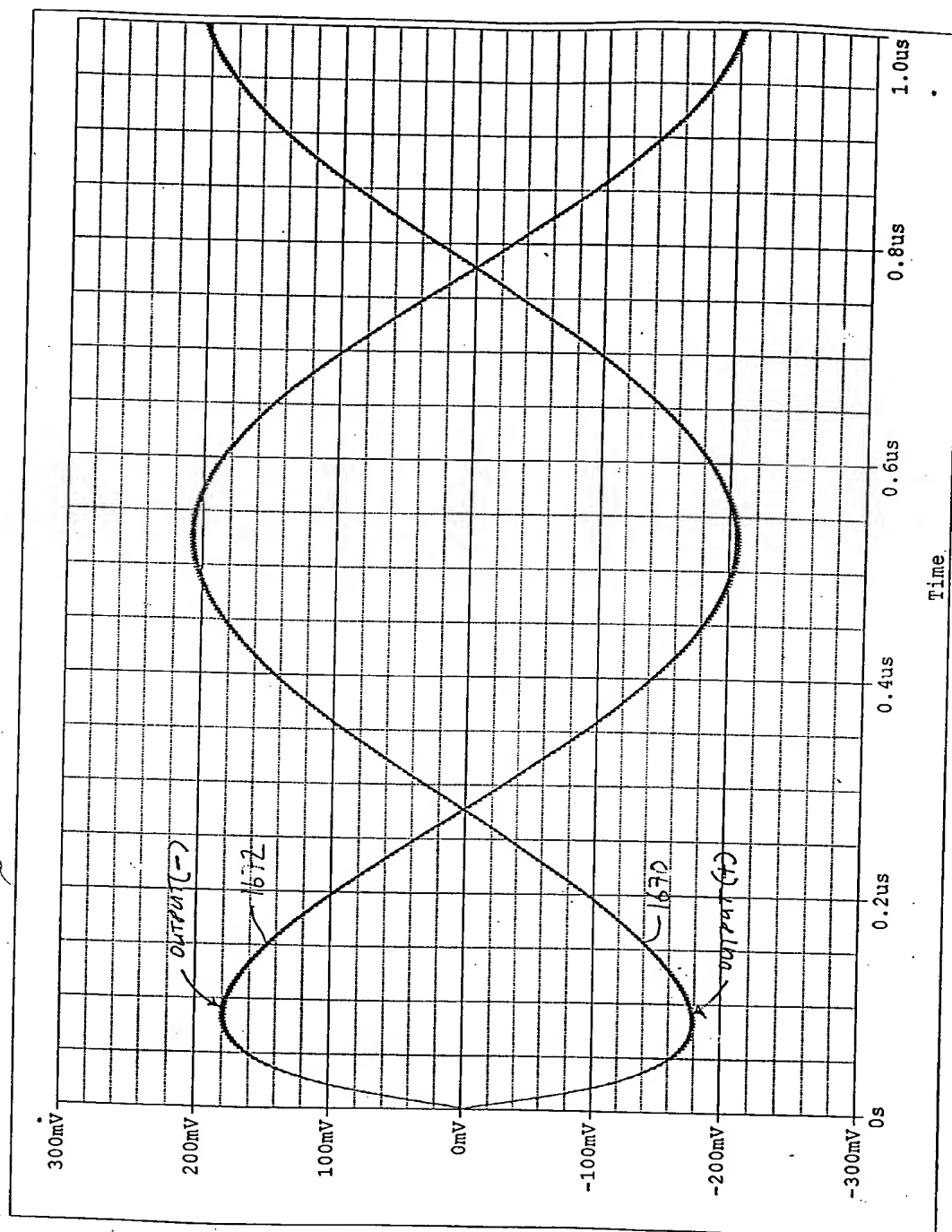


FIG. 16 G

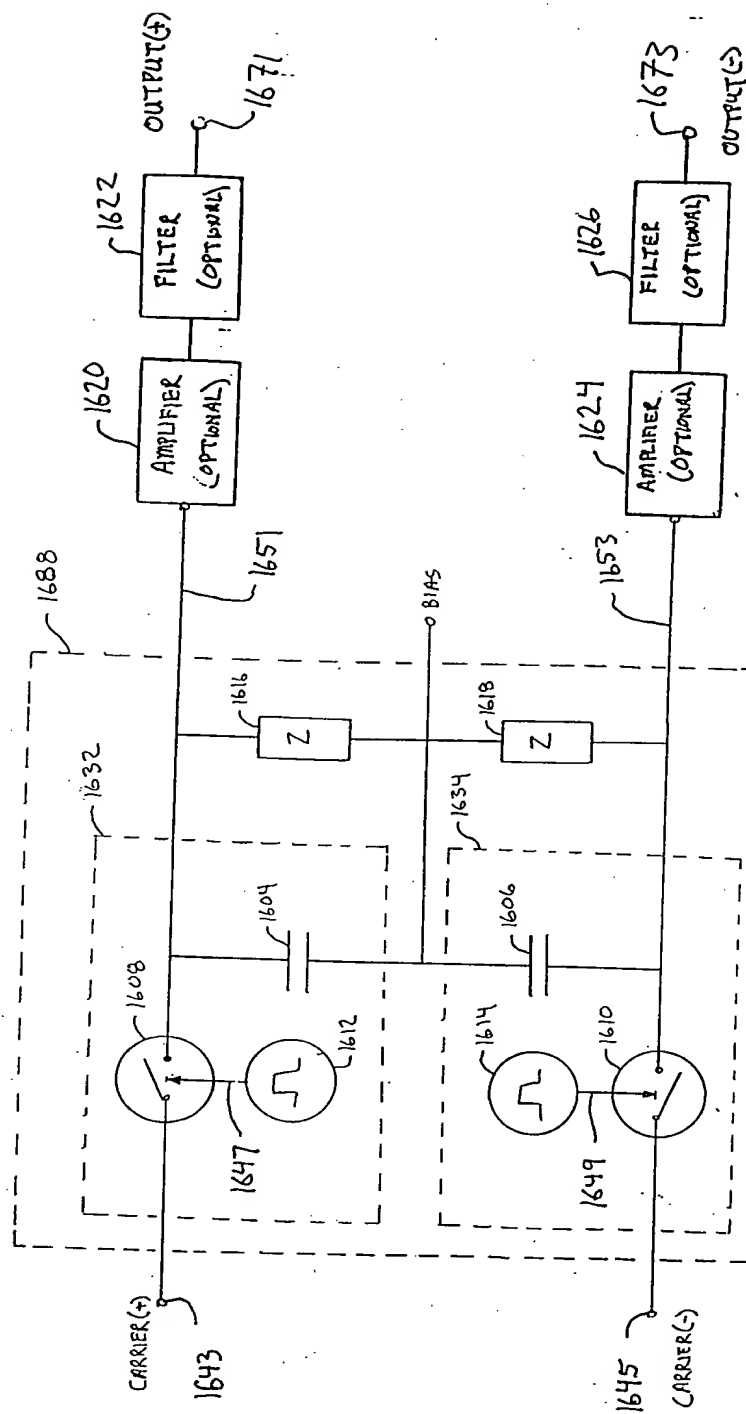


FIG. 16H

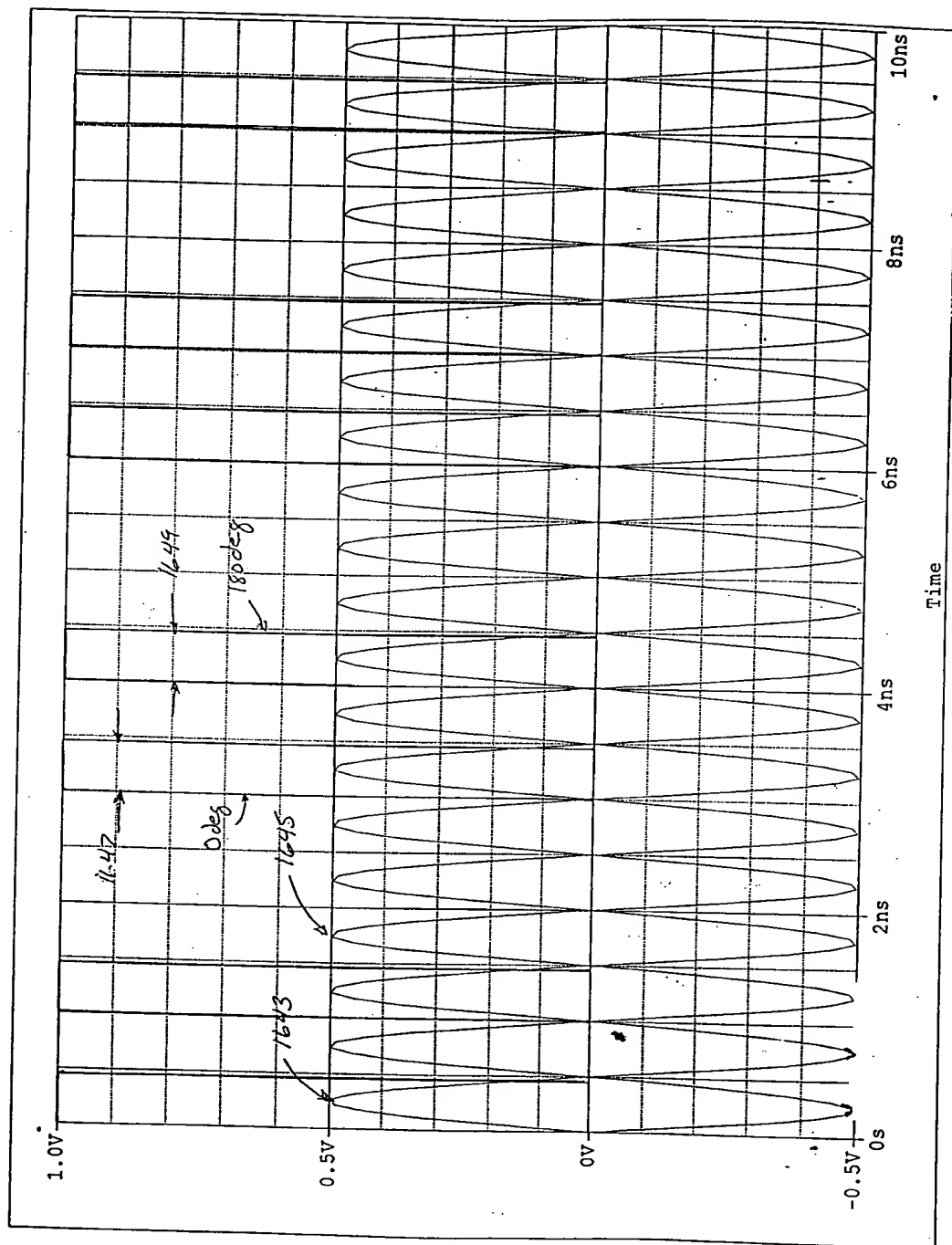


FIG. 16I

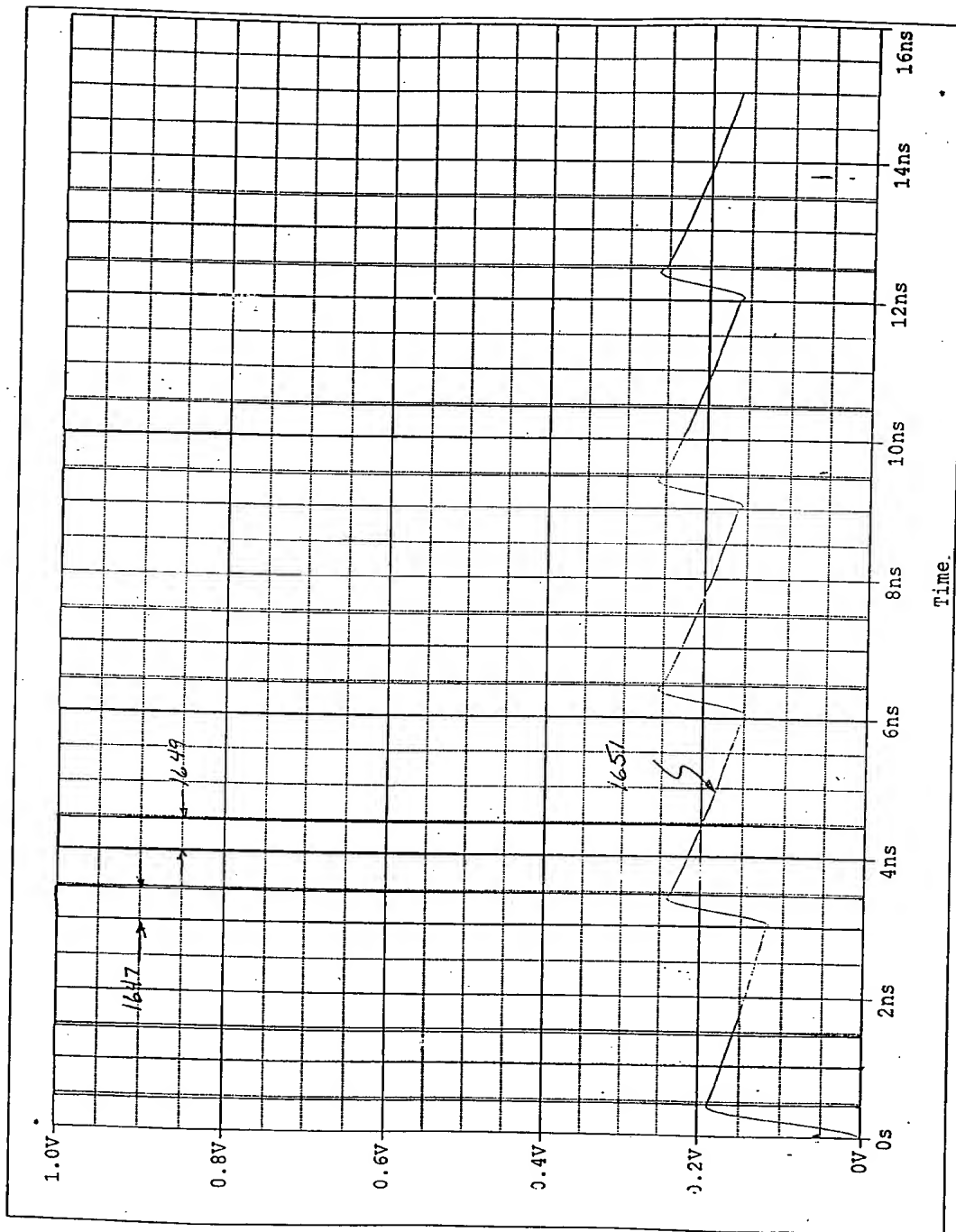


FIG 16J



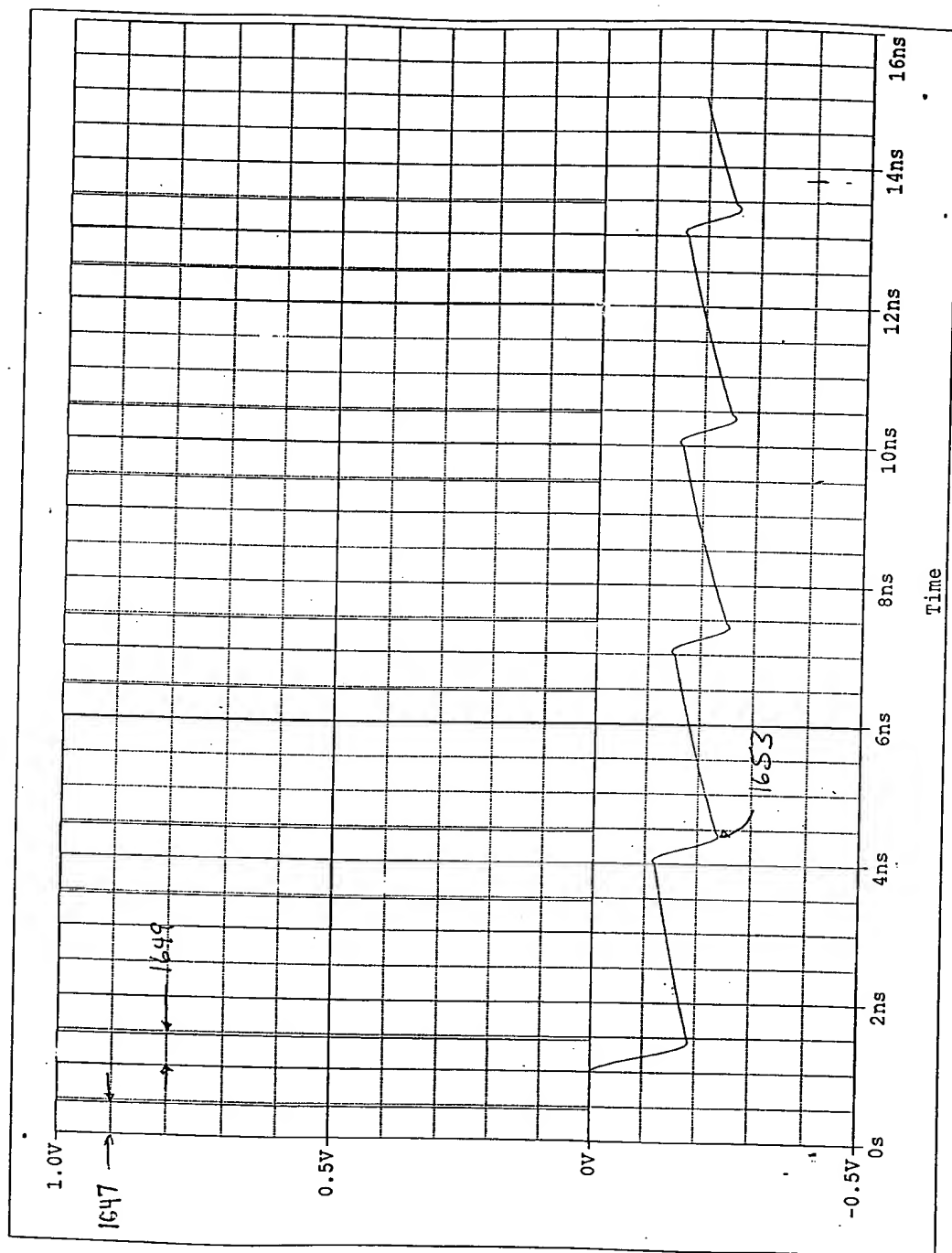


FIG. 16K

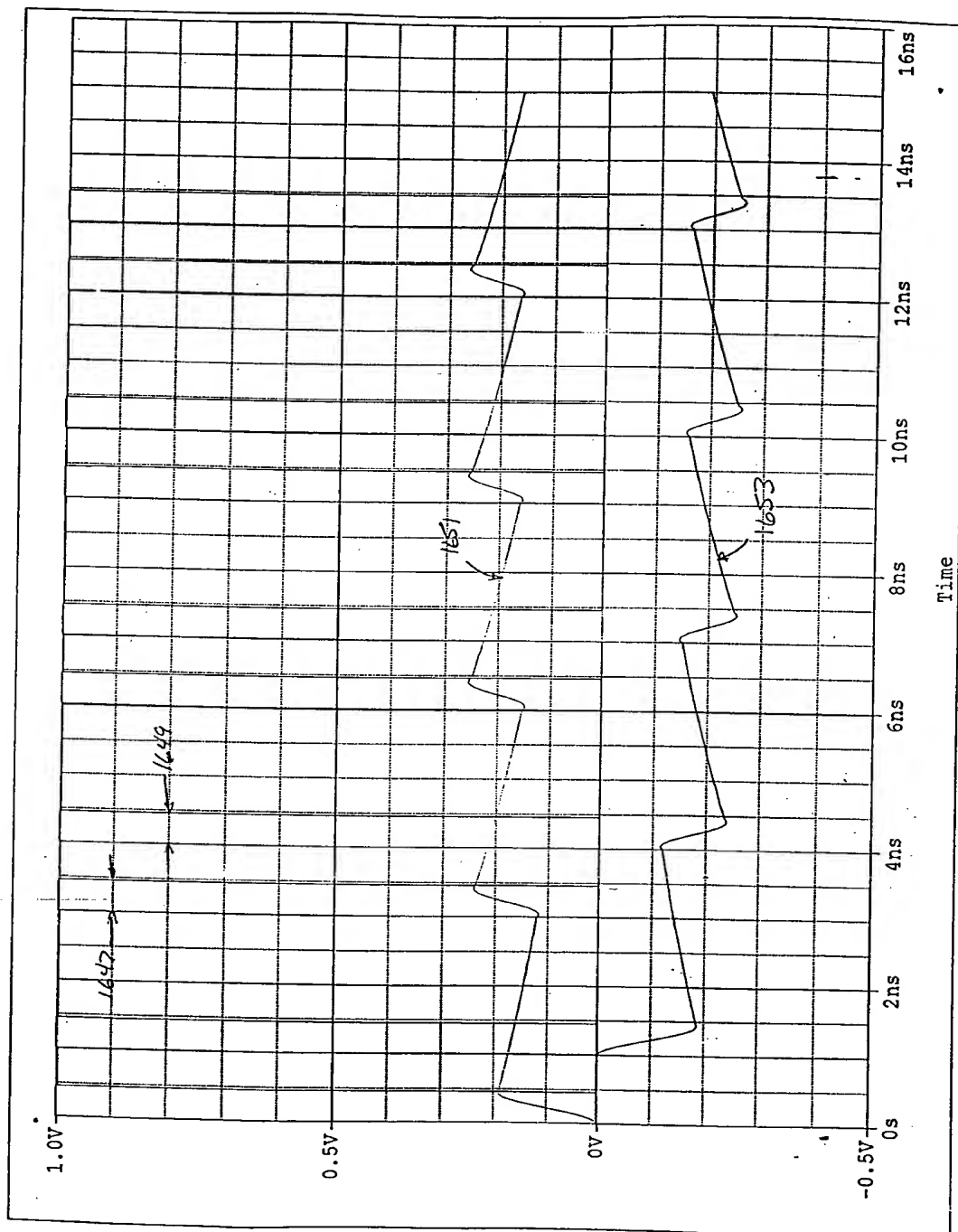


FIG. 16L

FO9T50" F5855860

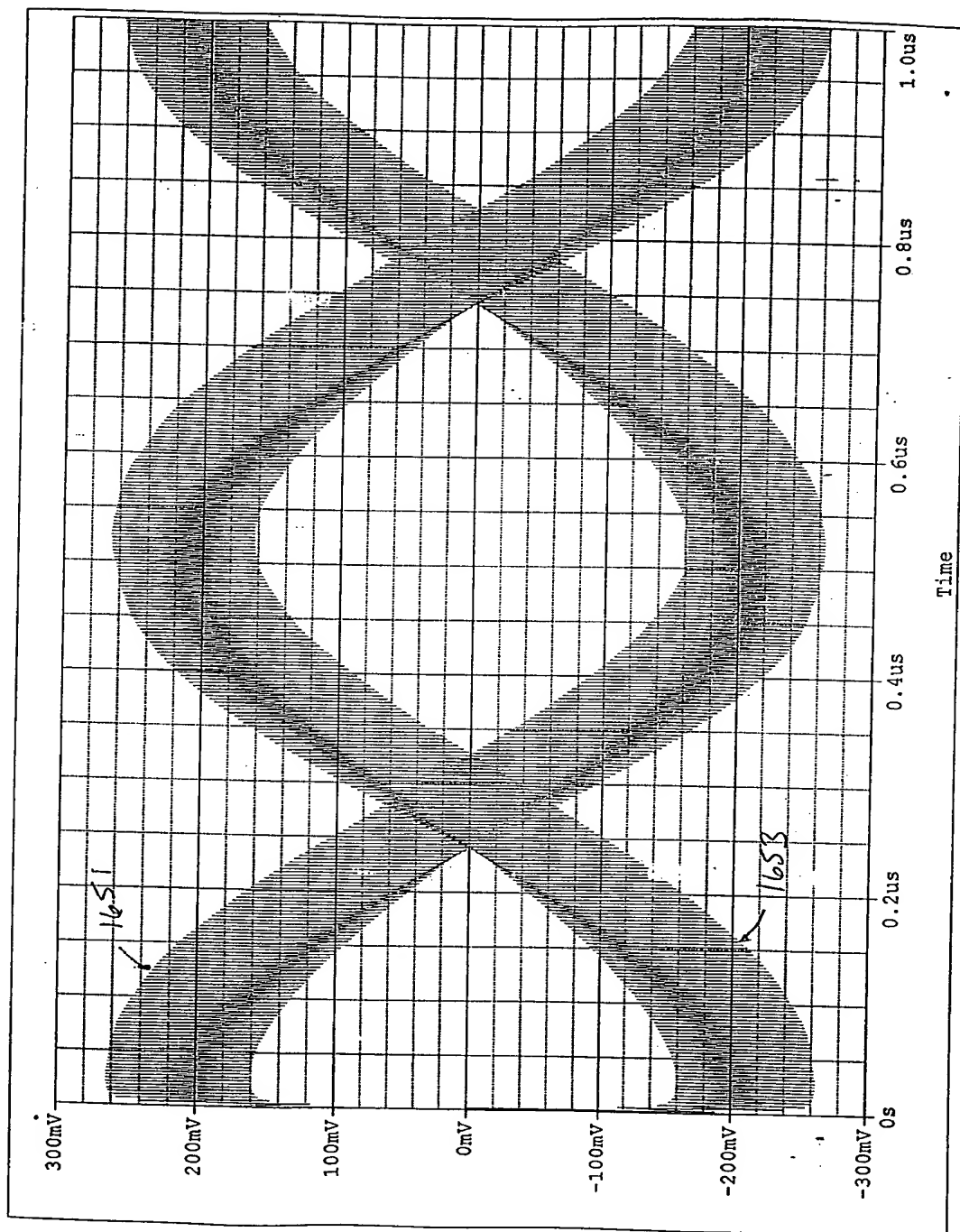


FIG. 16M

TOP SECRET 1585860

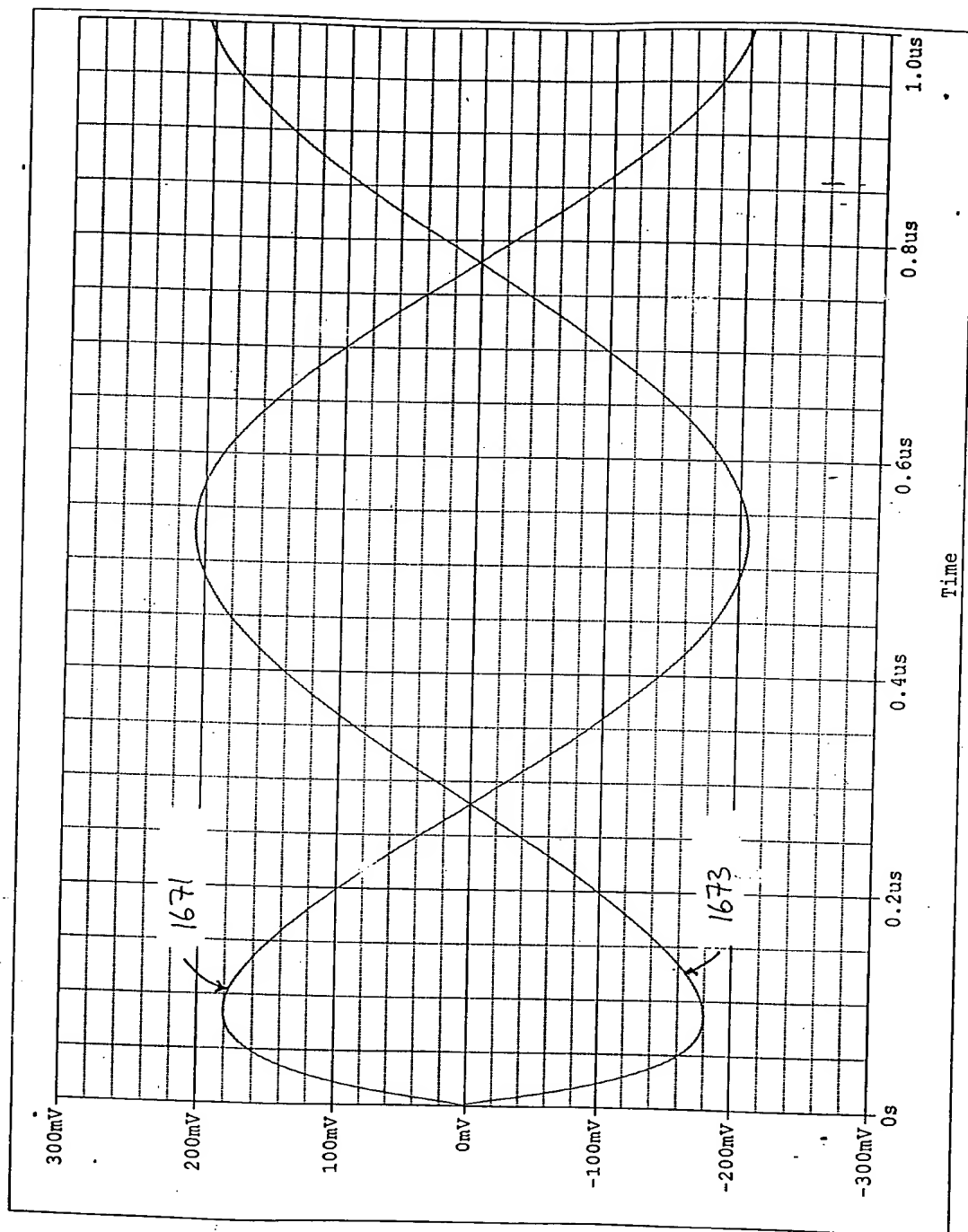


FIG. 16N

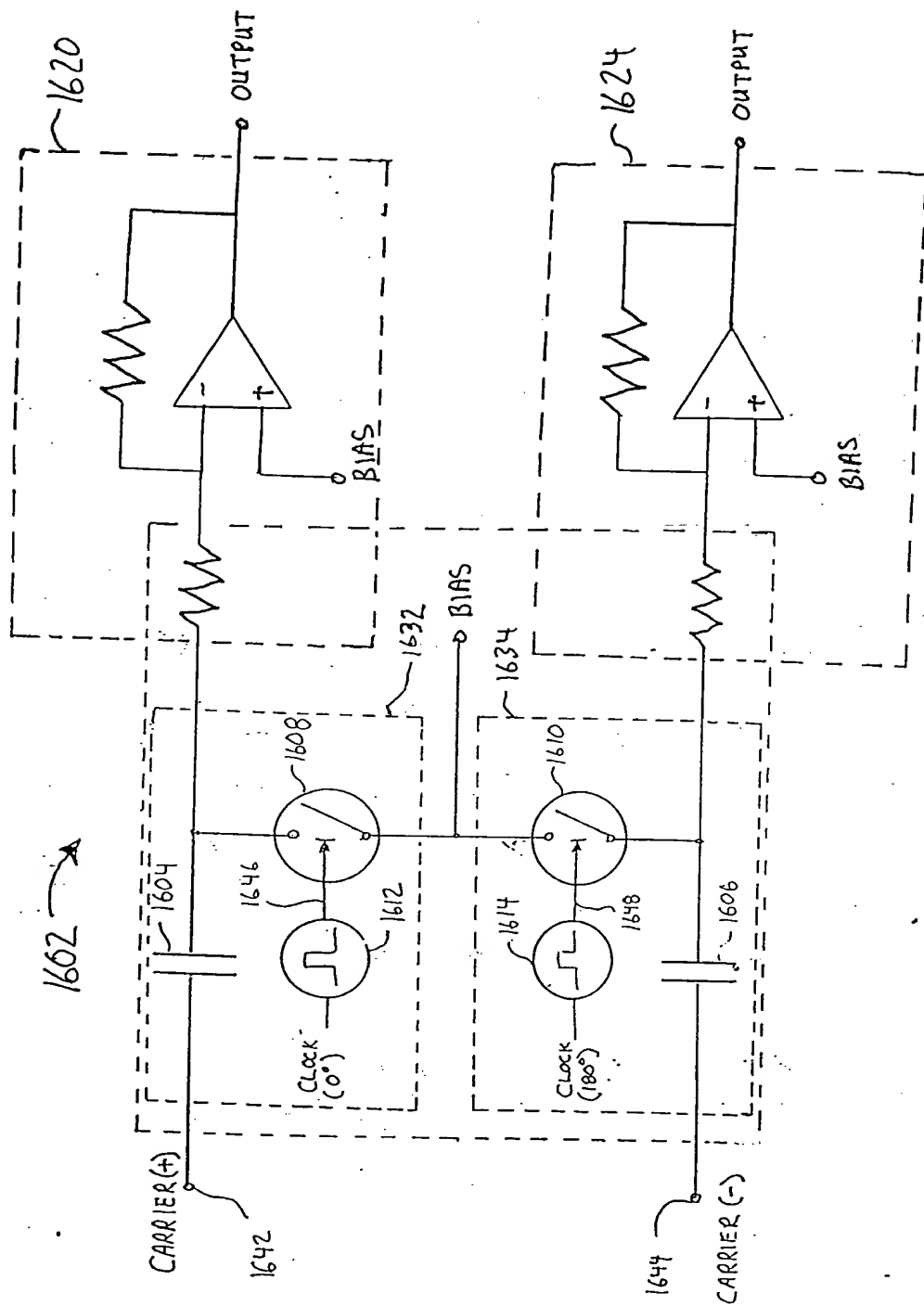


FIG. 160

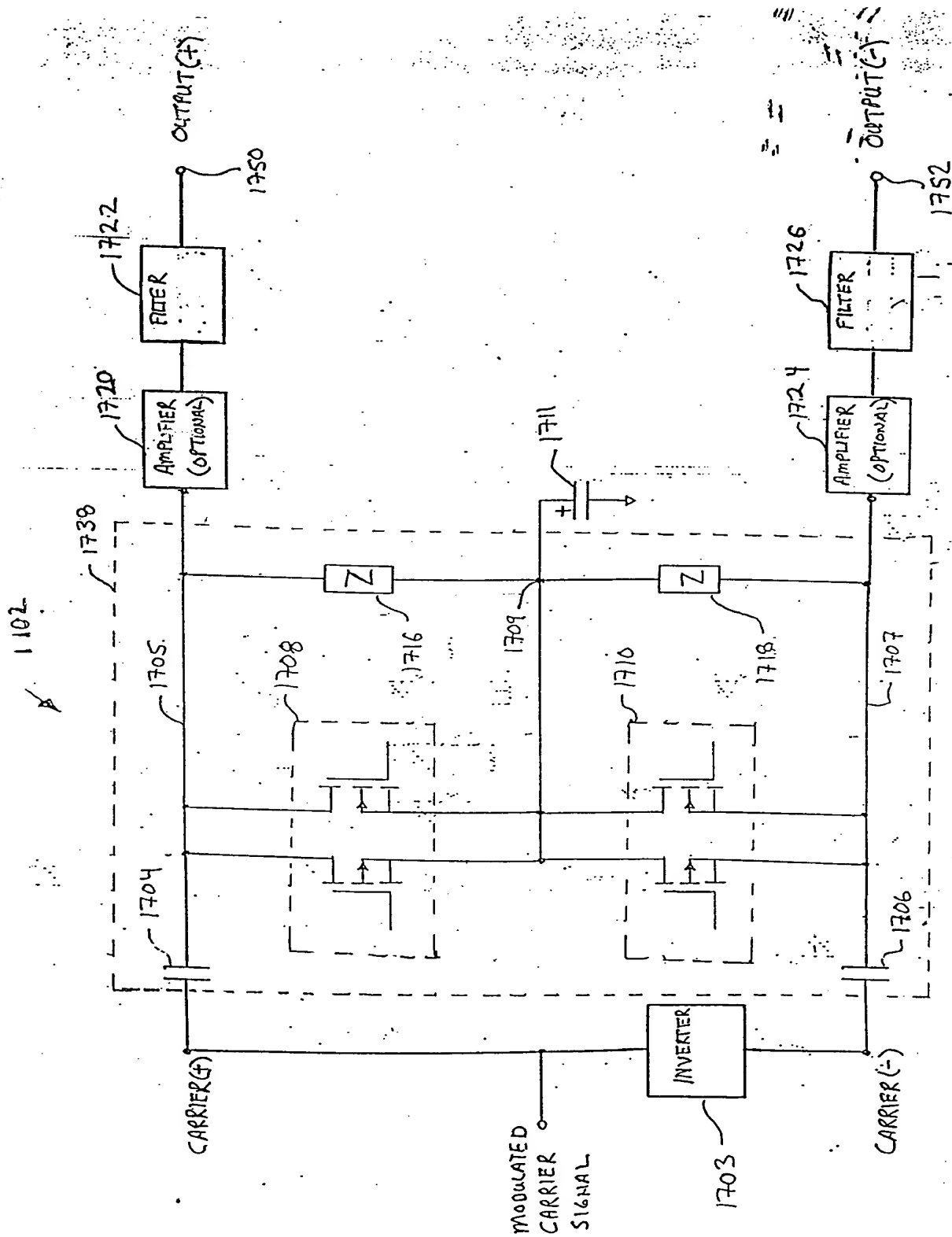
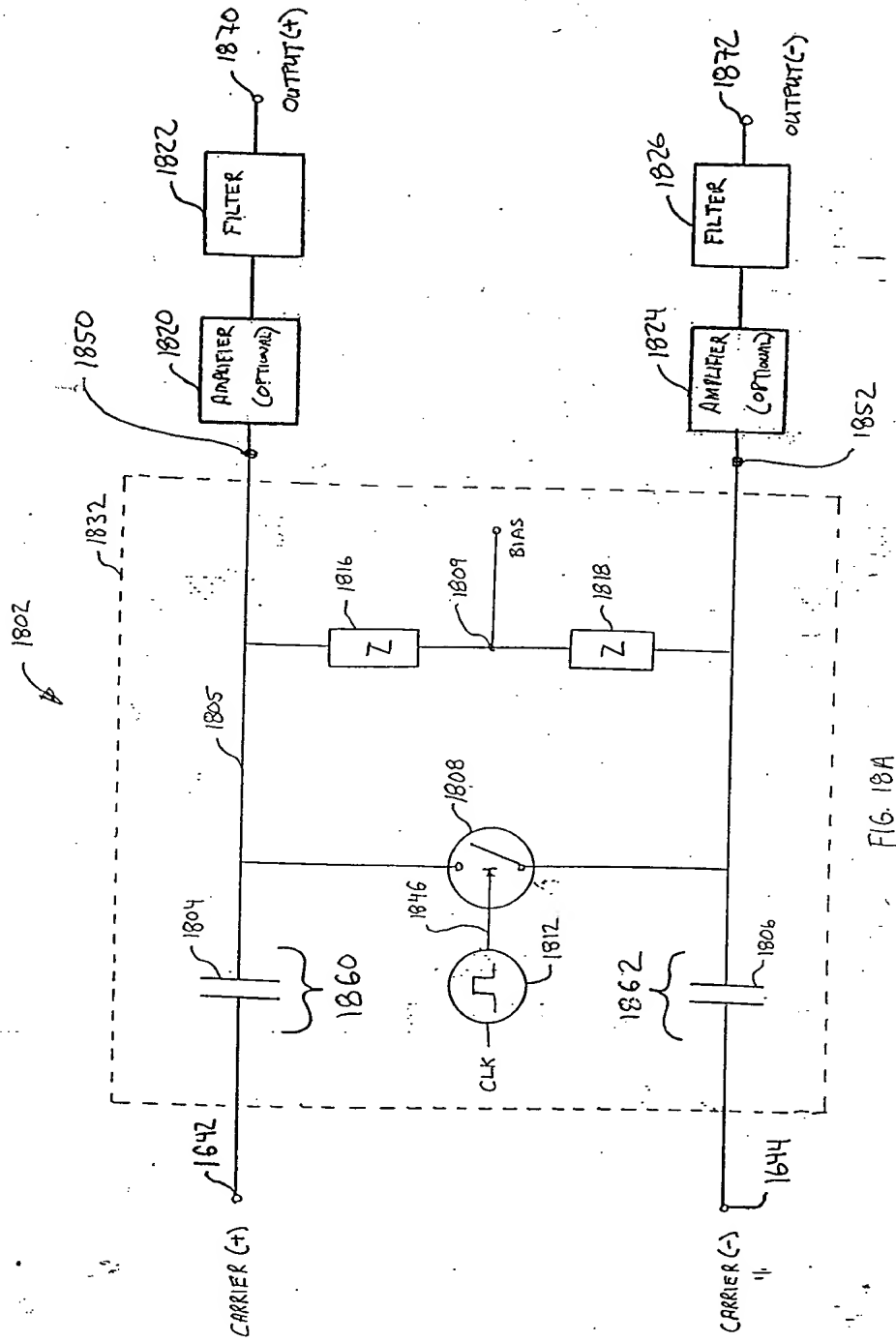


FIG. 17



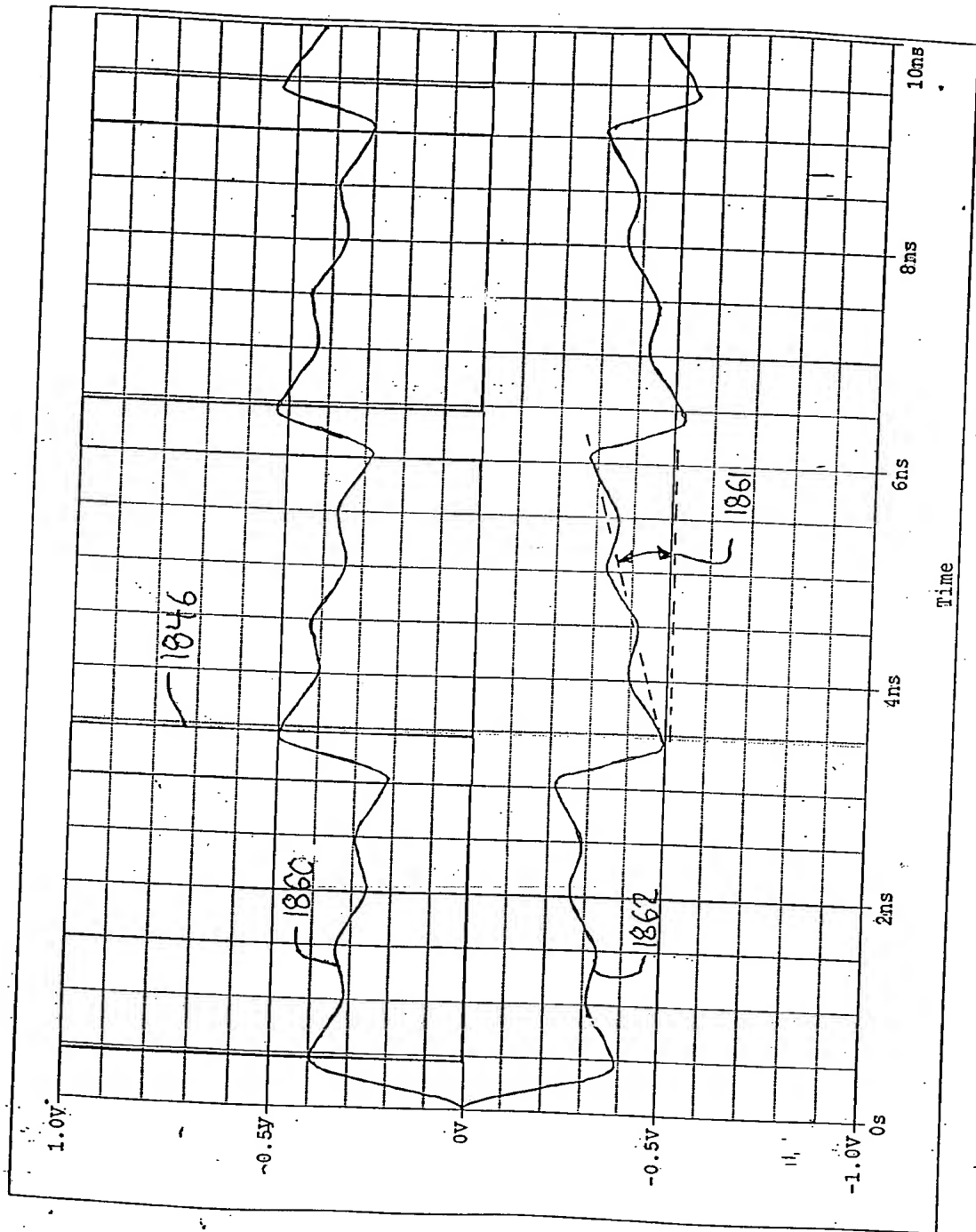


FIG. 18B



09555860

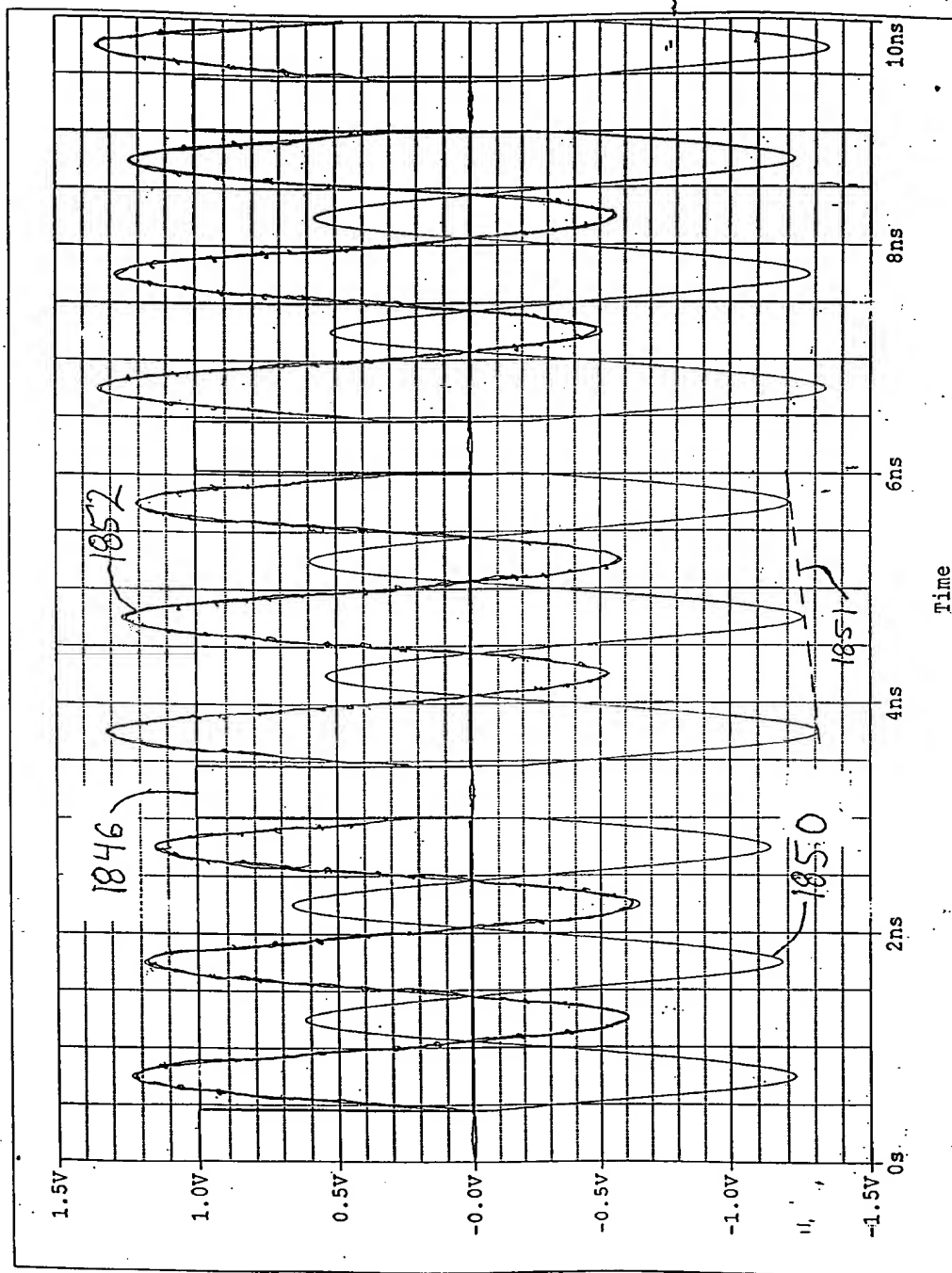


FIG. 18C

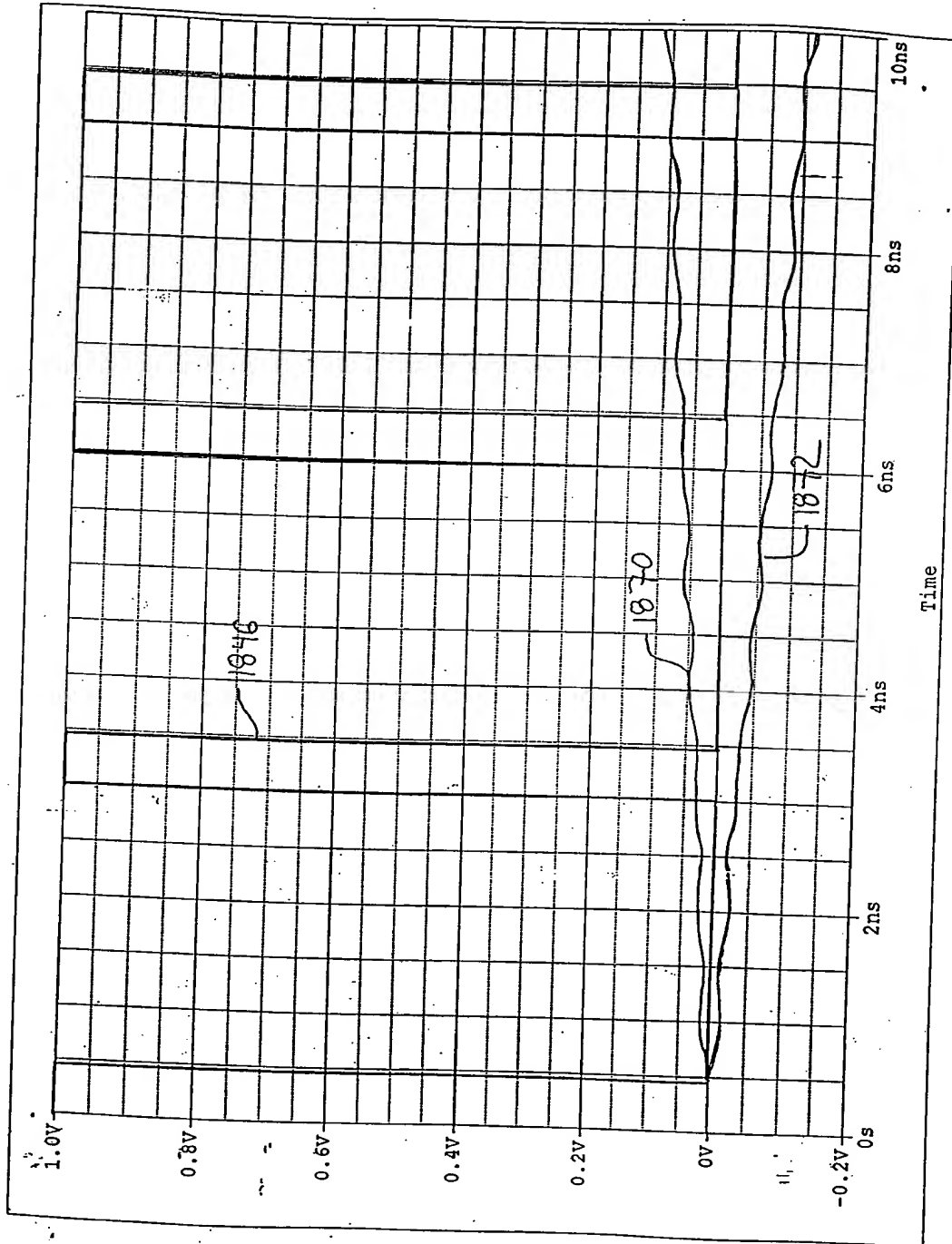


FIG. 18D

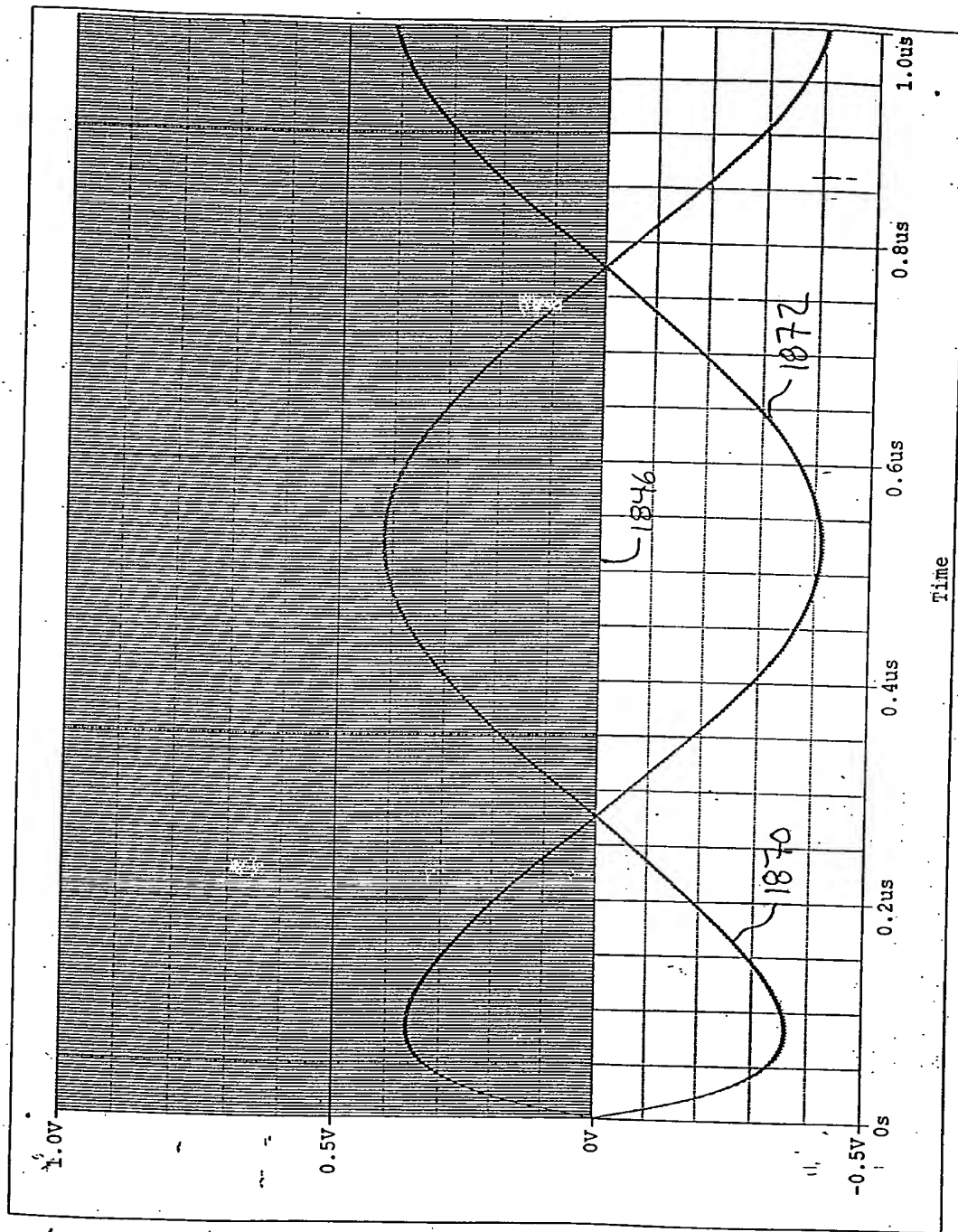


FIG. 18E

1902

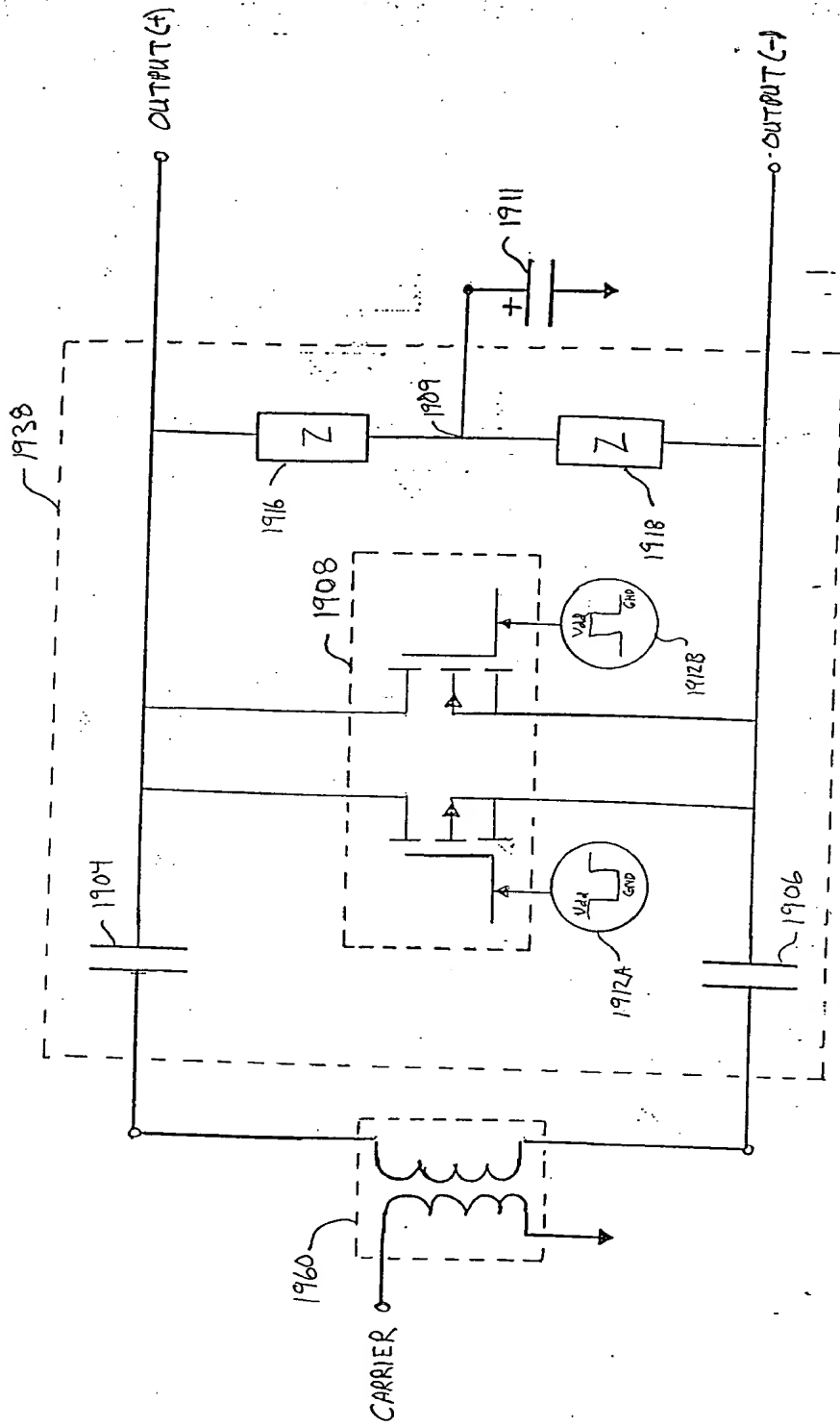


FIG. 19

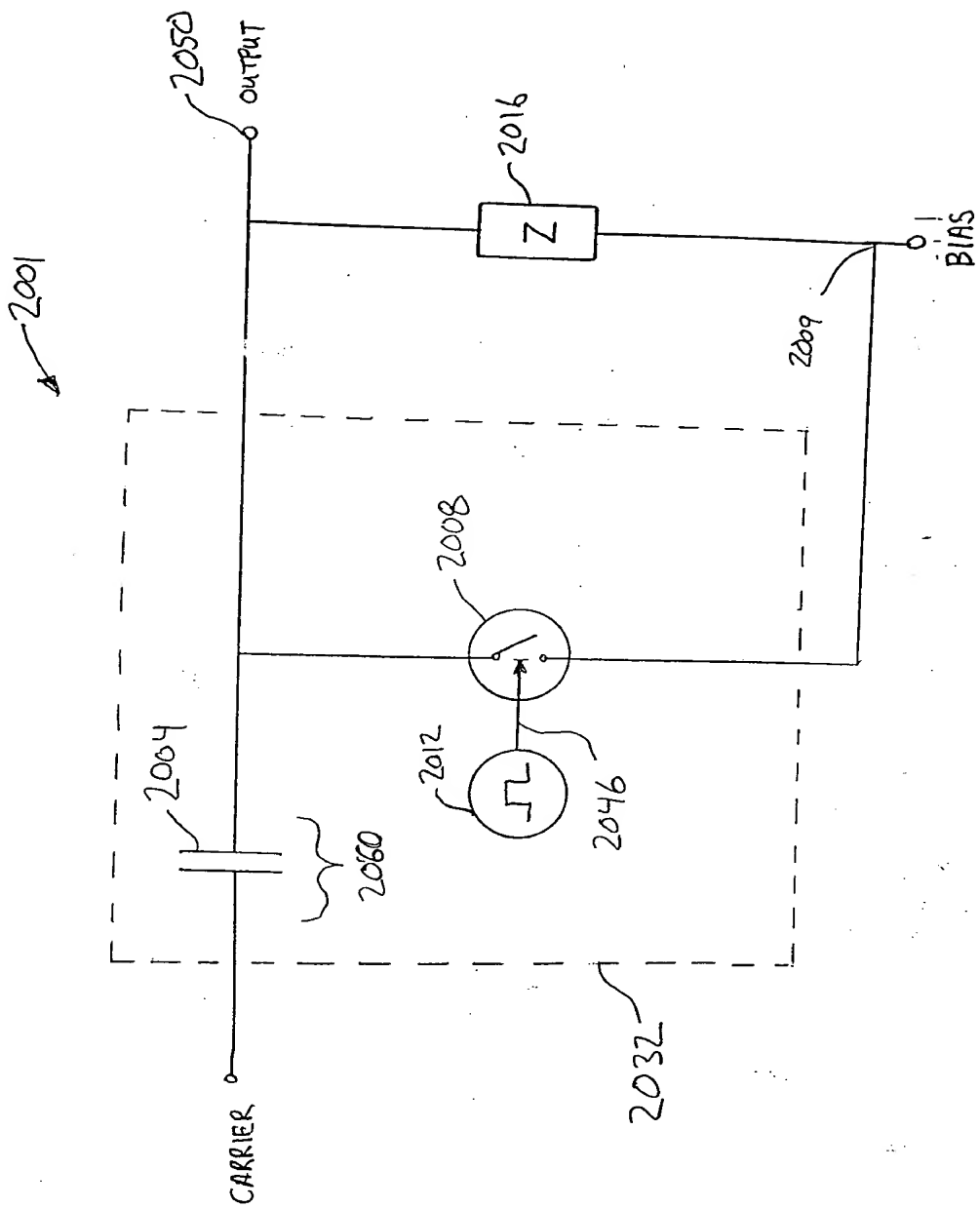


FIG. 20A

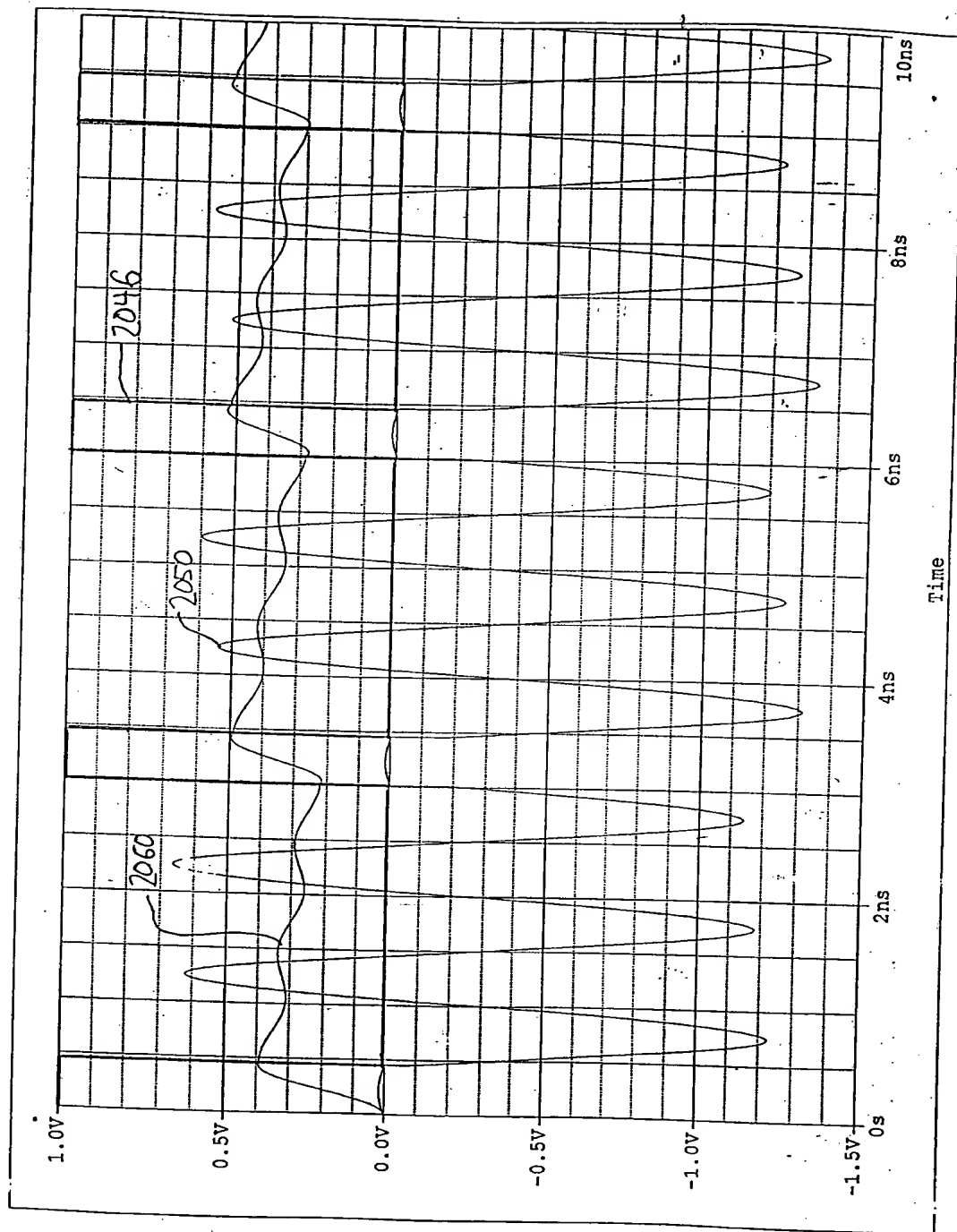


FIG. 20B

095531 0460 15855860

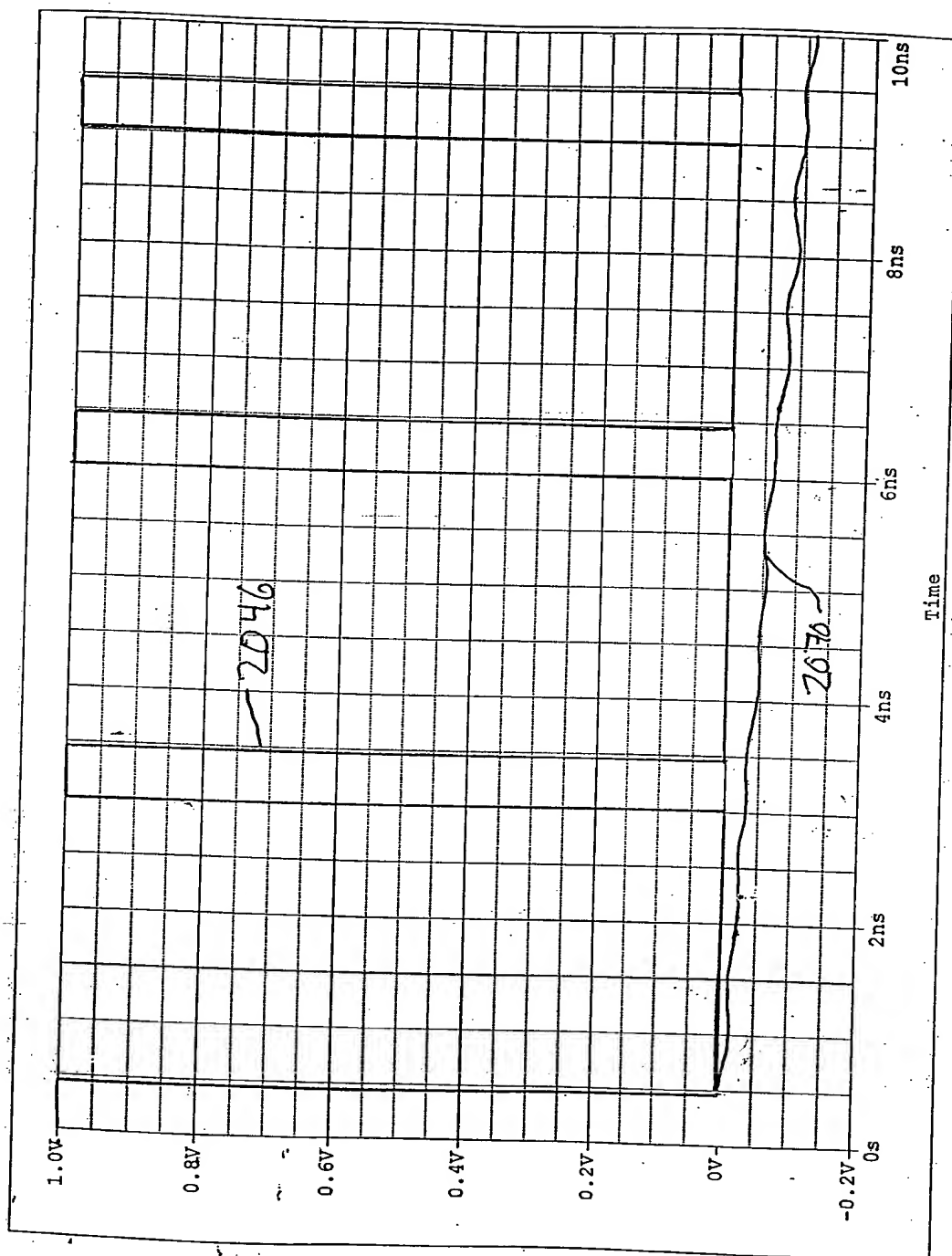


FIG. 20C

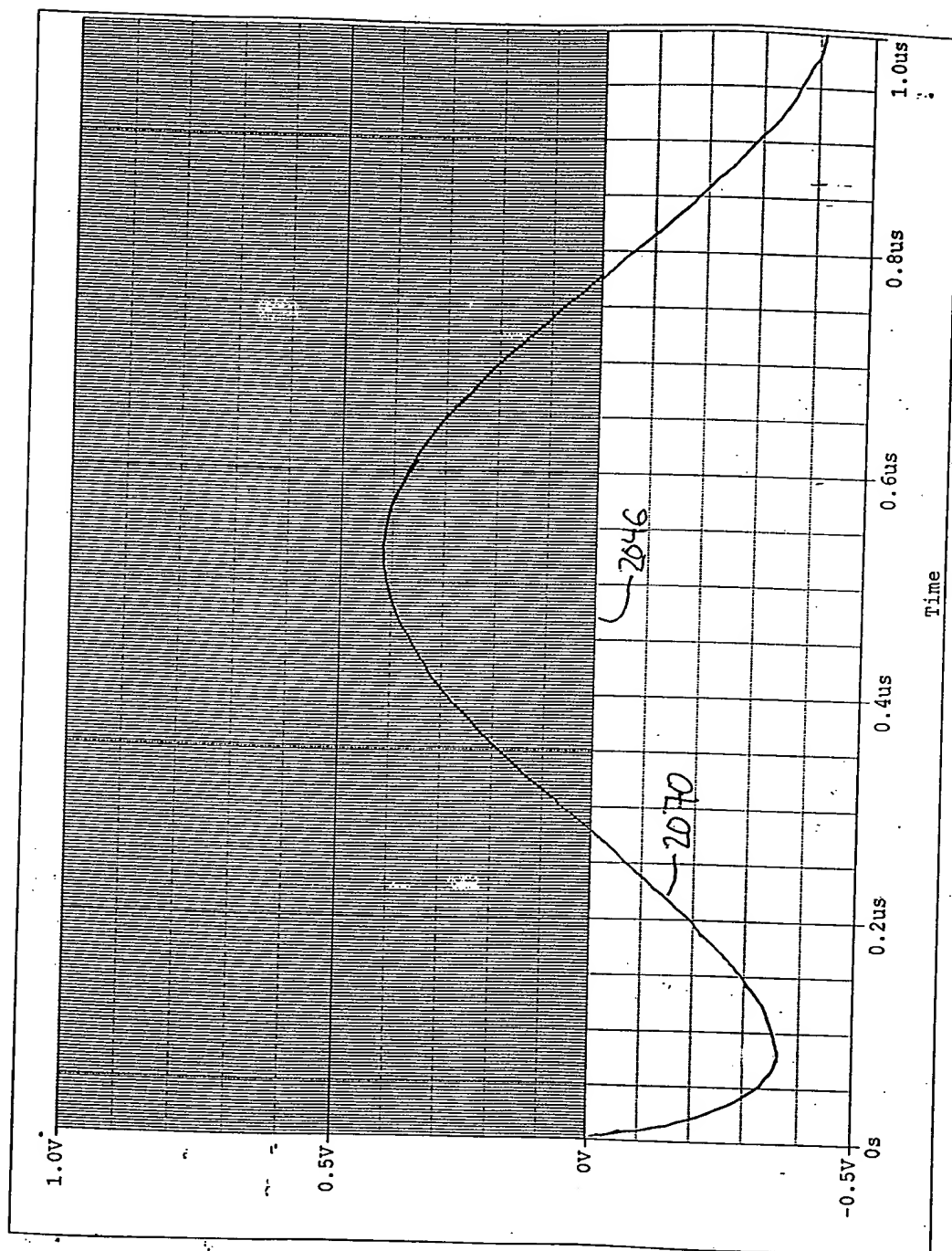


FIG. 20D



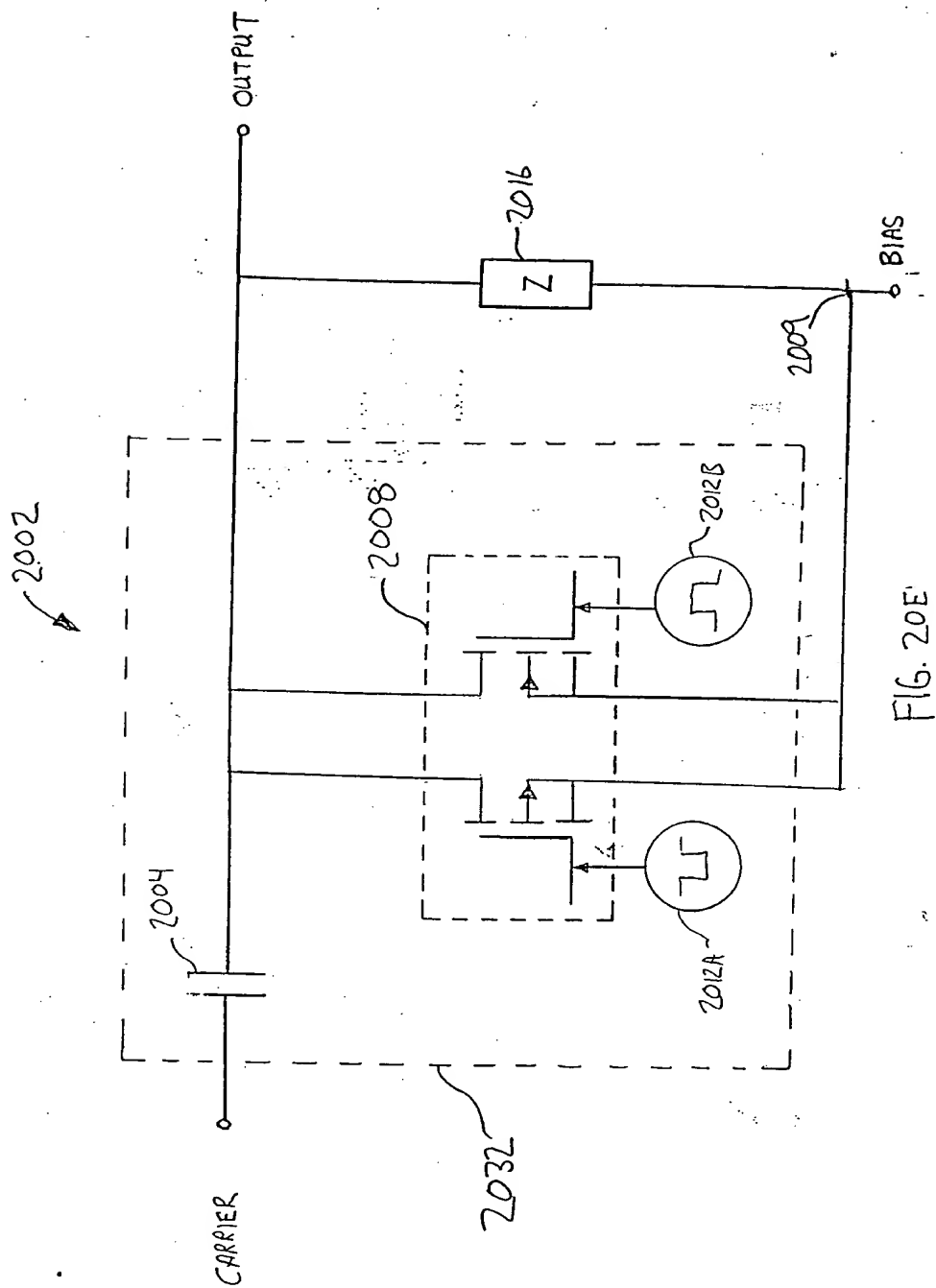


FIG. 20E

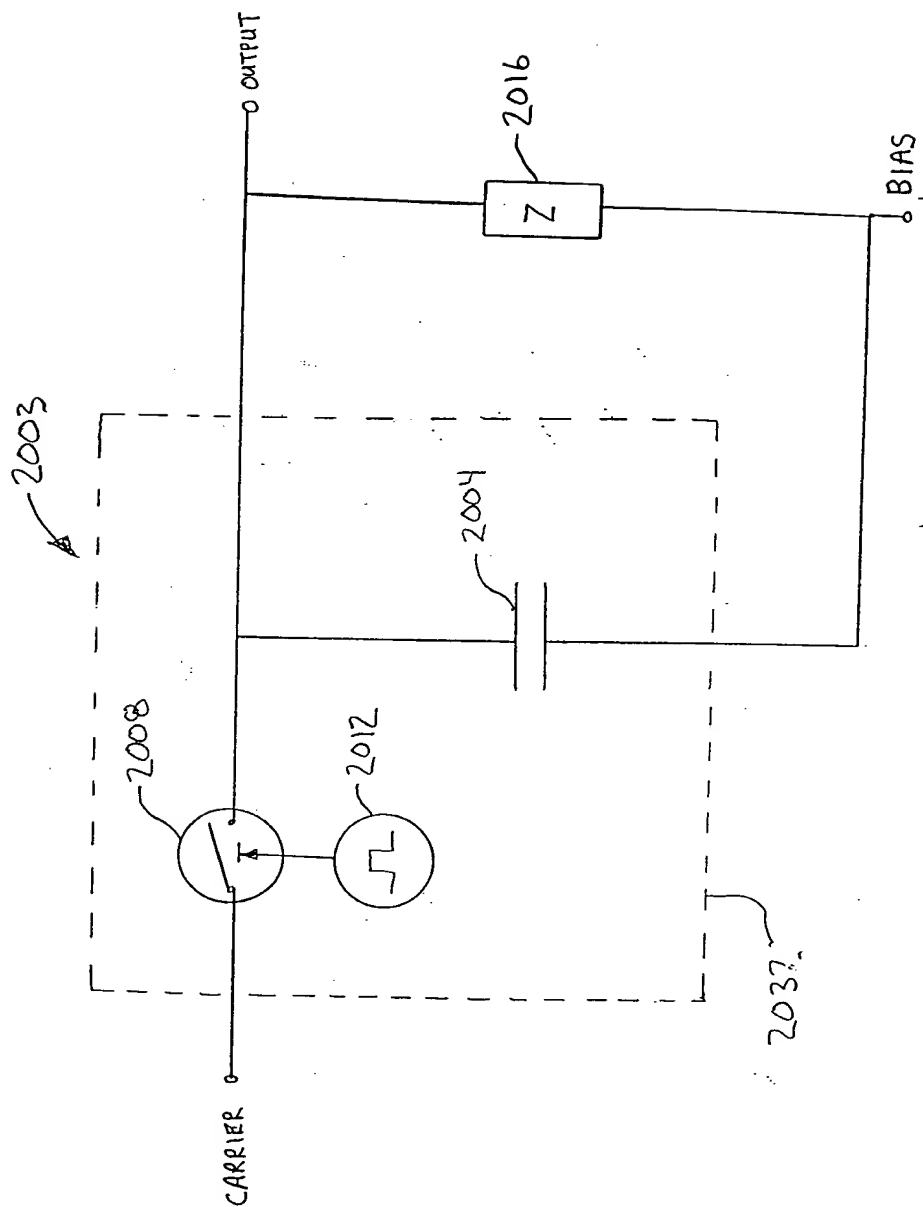


FIG. 20F

2101

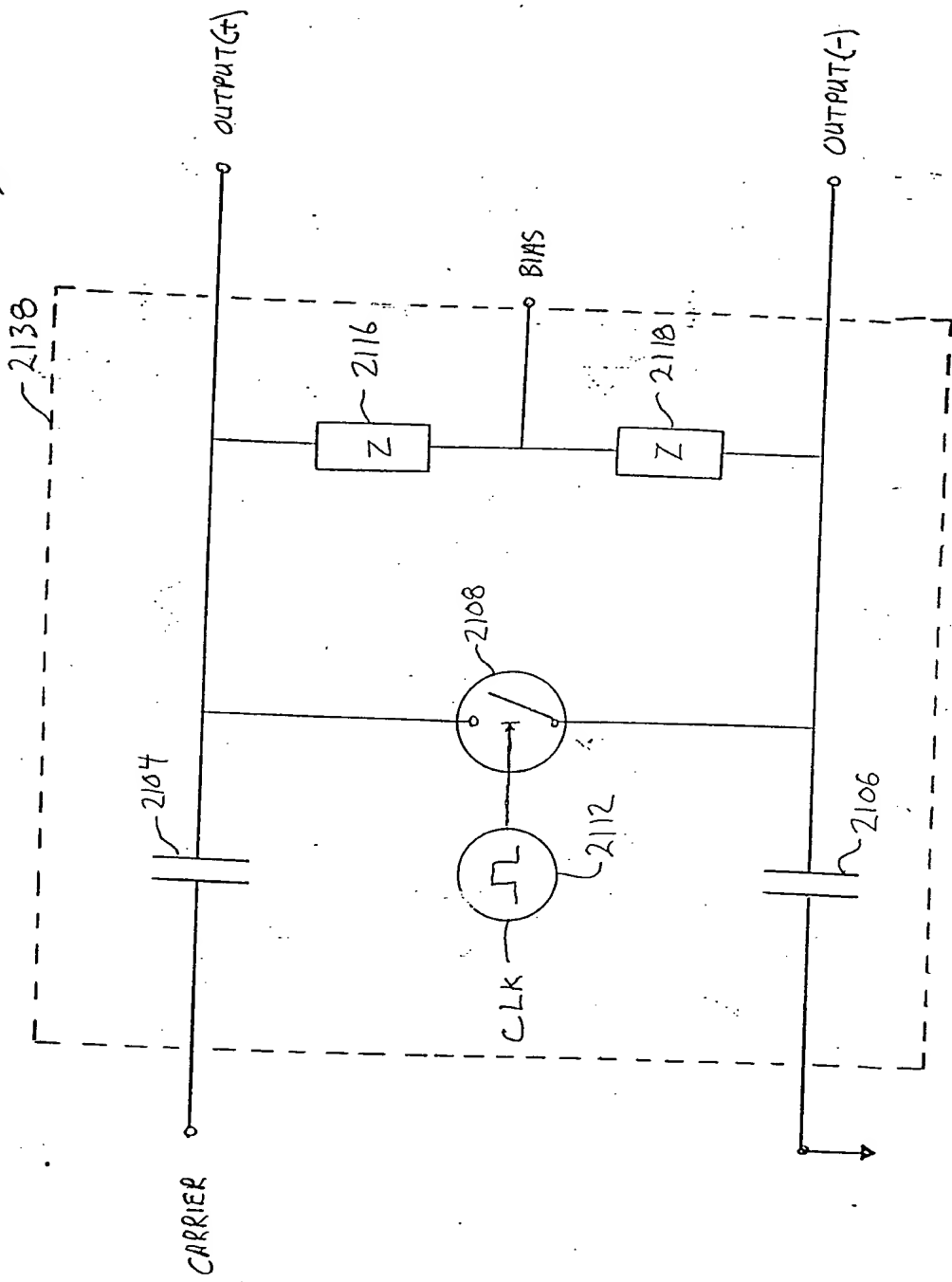


FIG. 21

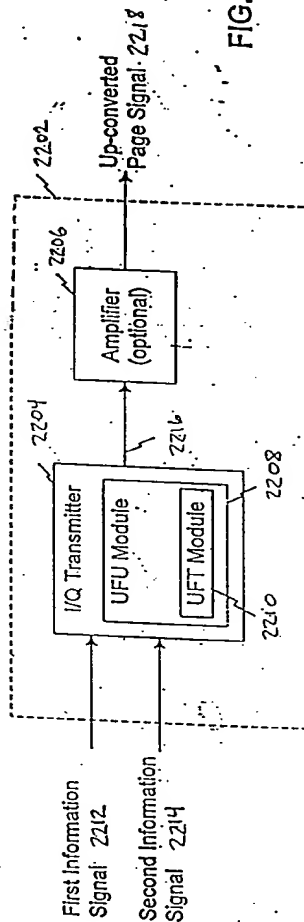


FIG. 22

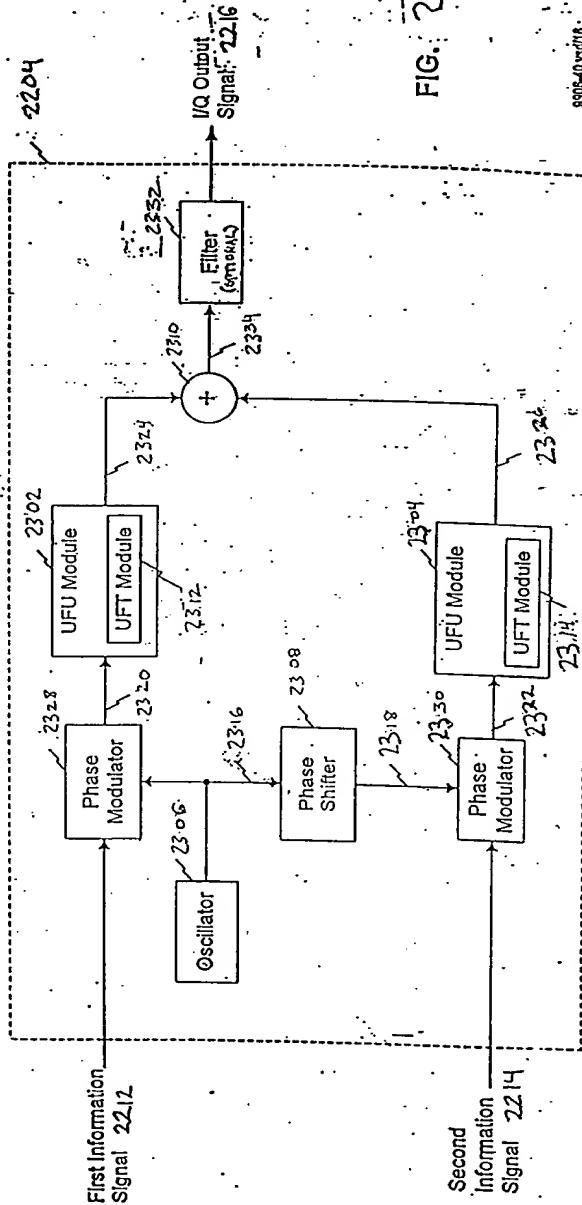


FIG. 23

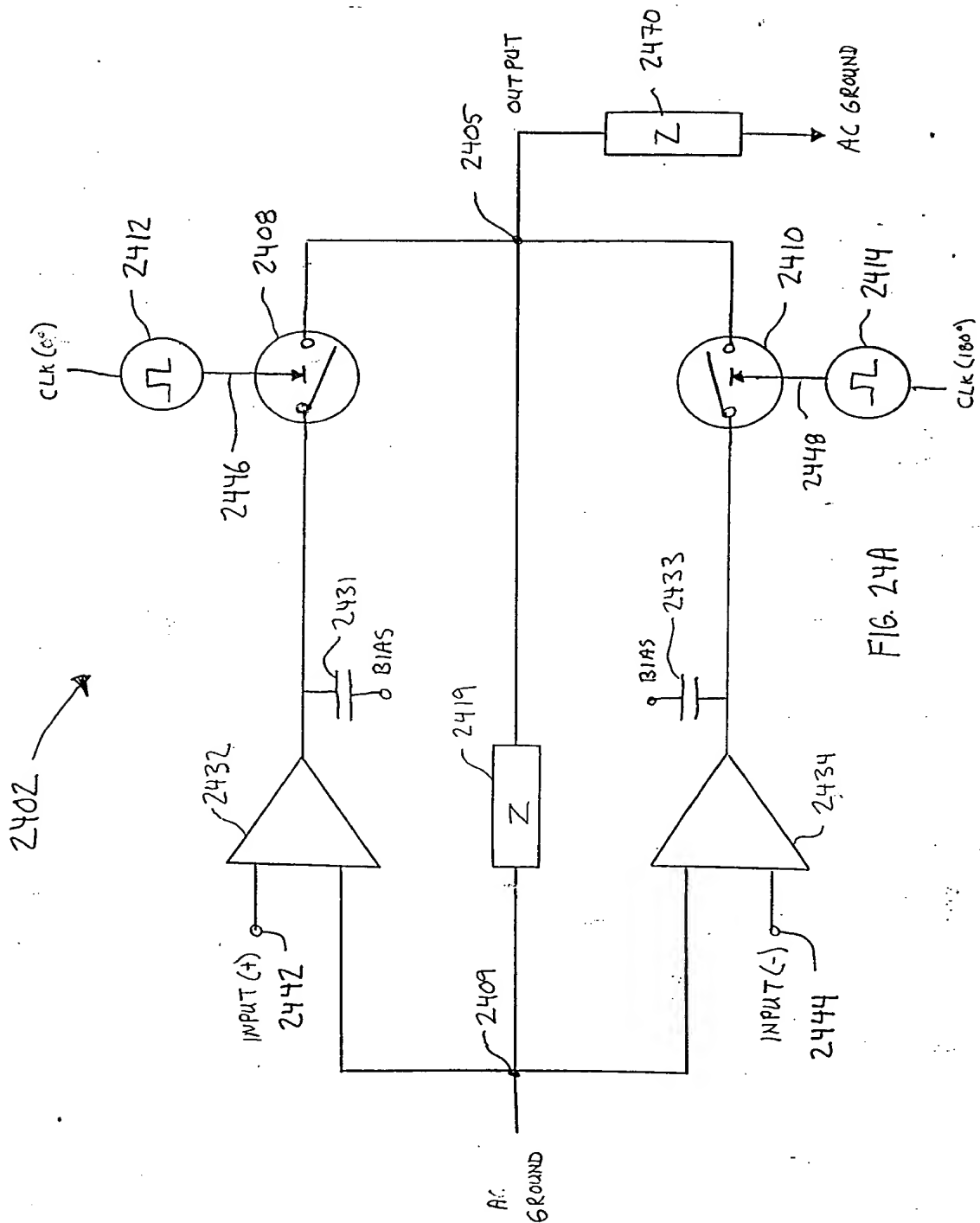
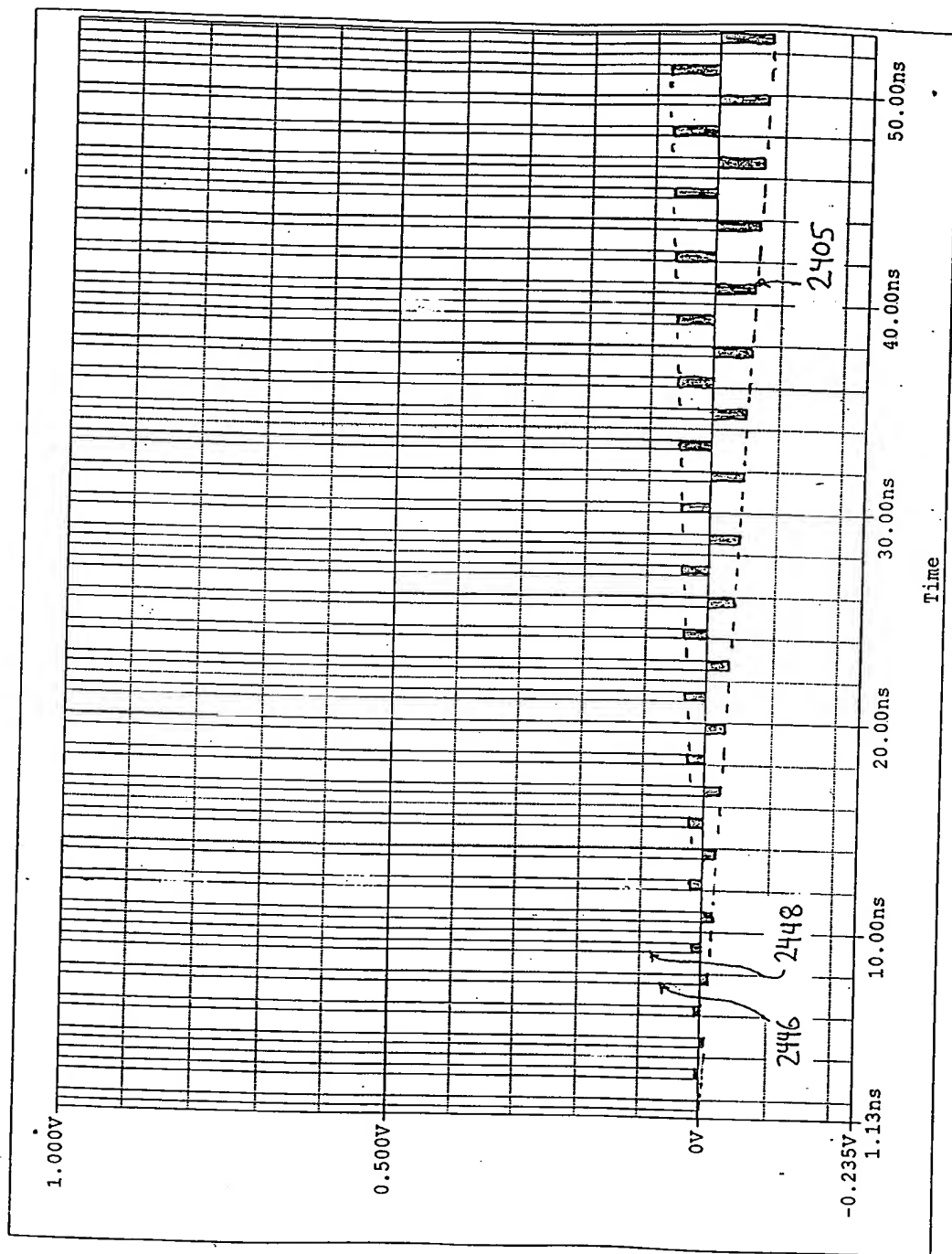


FIG. 24A

TOP SECRET



F16.24B

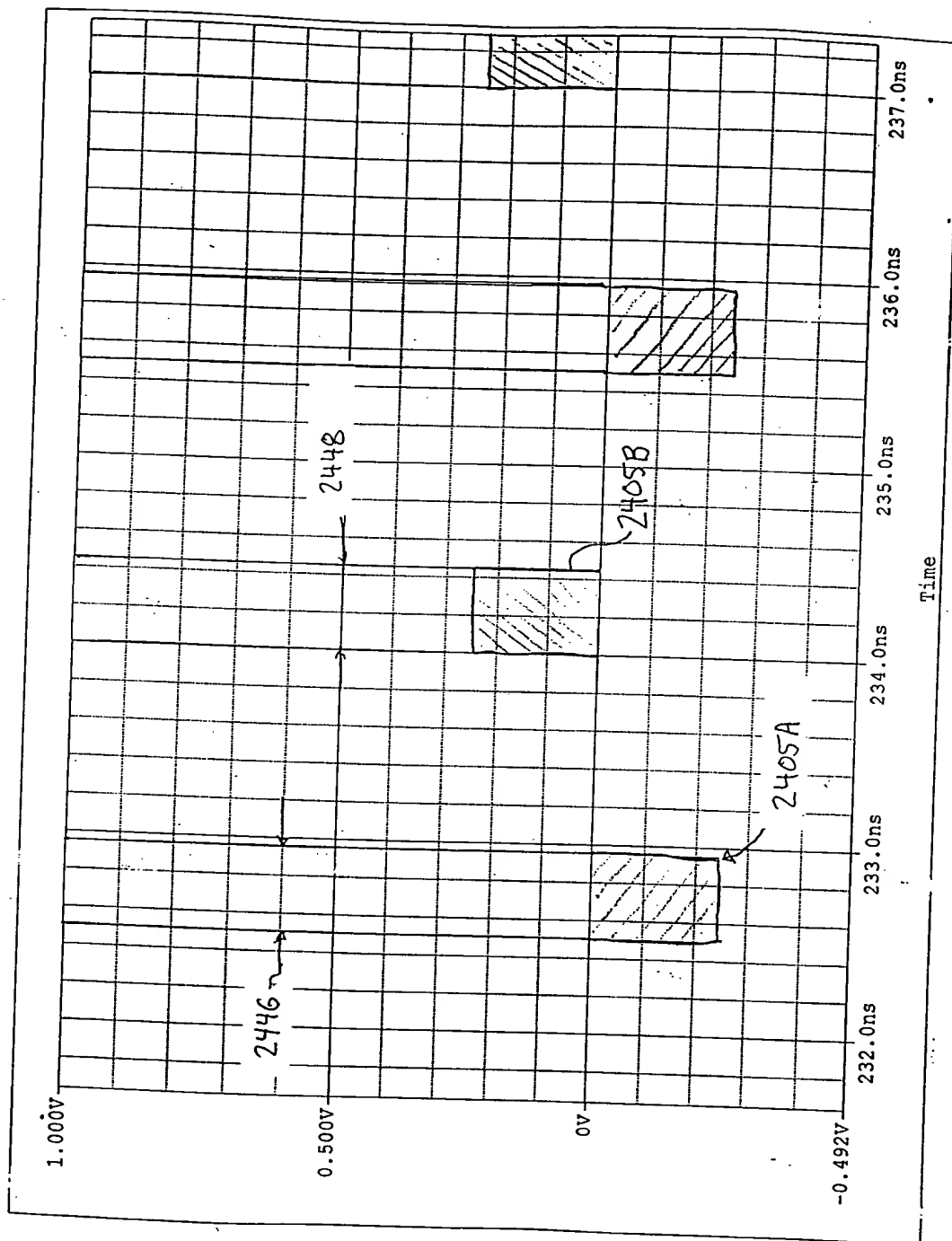


FIG. 24C

T09T50" T5855860

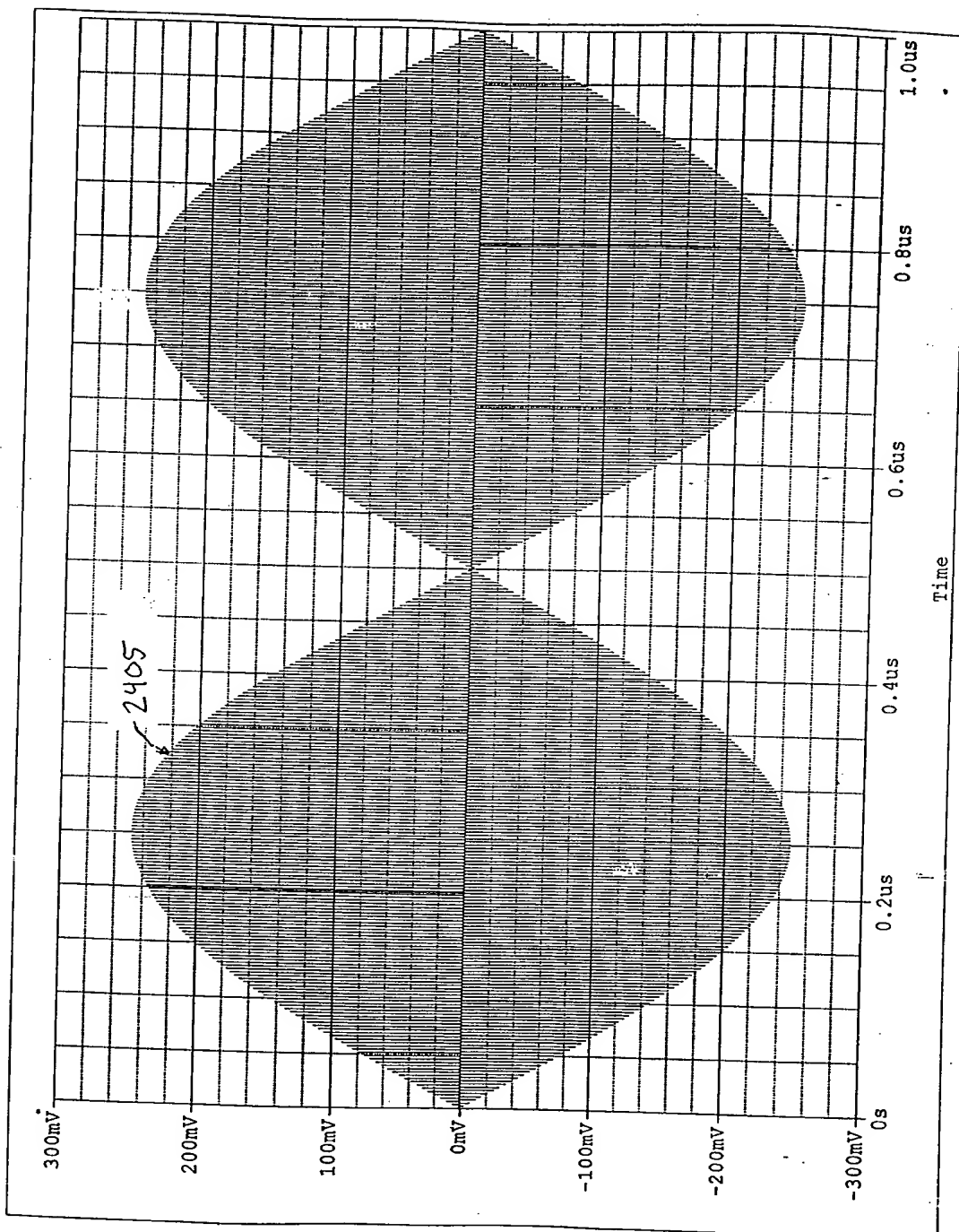


FIG. 24D



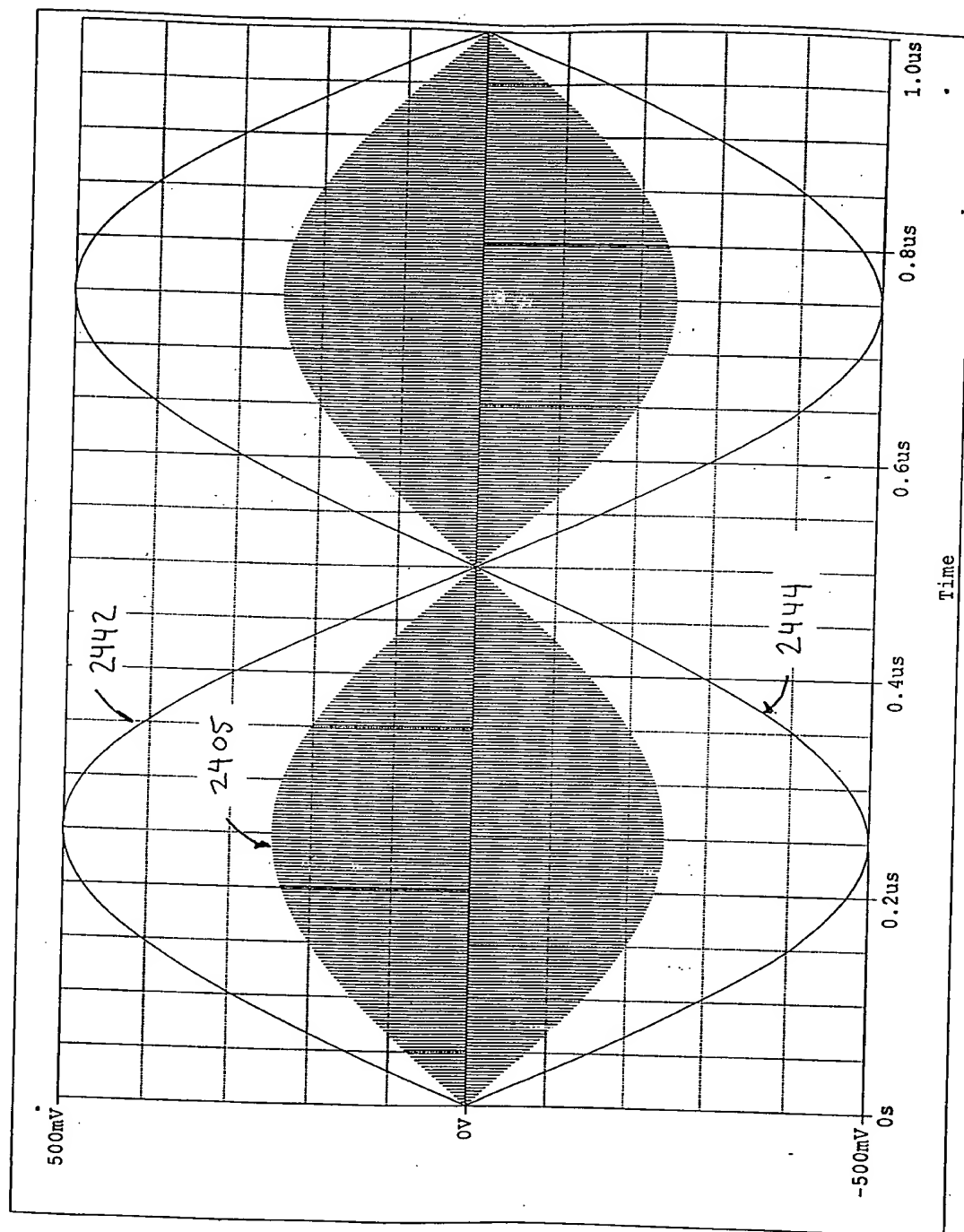


FIG. 24E

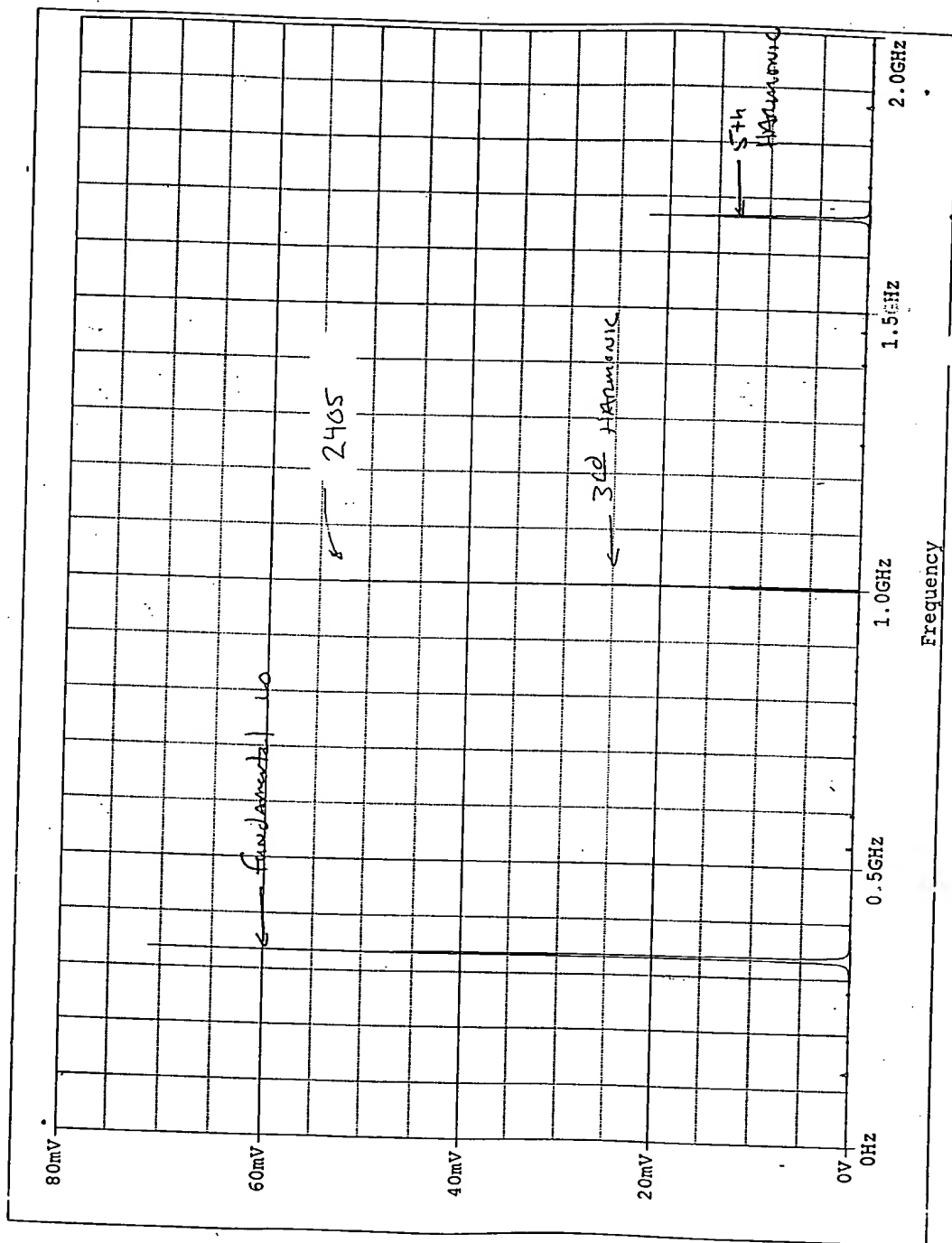


FIG. 24 F

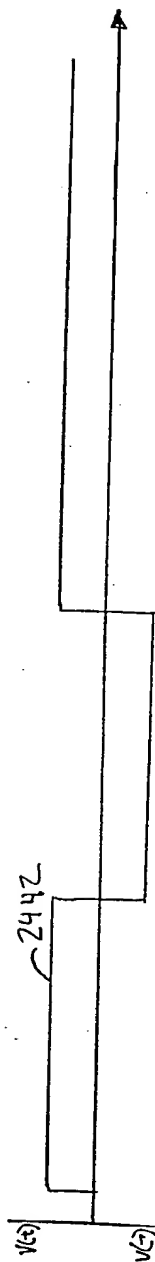


FIG. 24 G

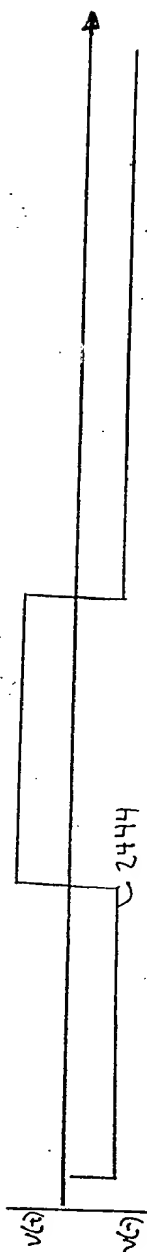


FIG. 24 H

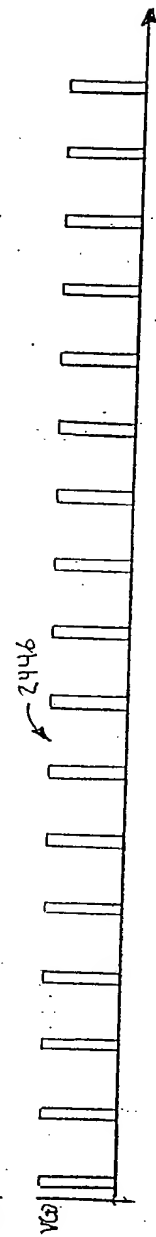


FIG. 24 I

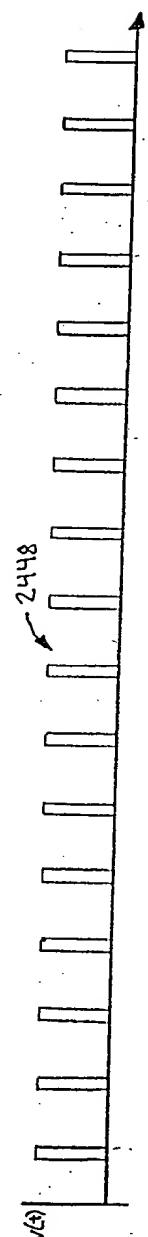


FIG. 24 J

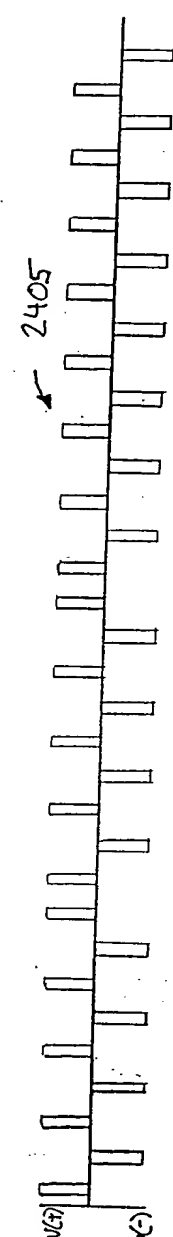


FIG. 24 K

2502

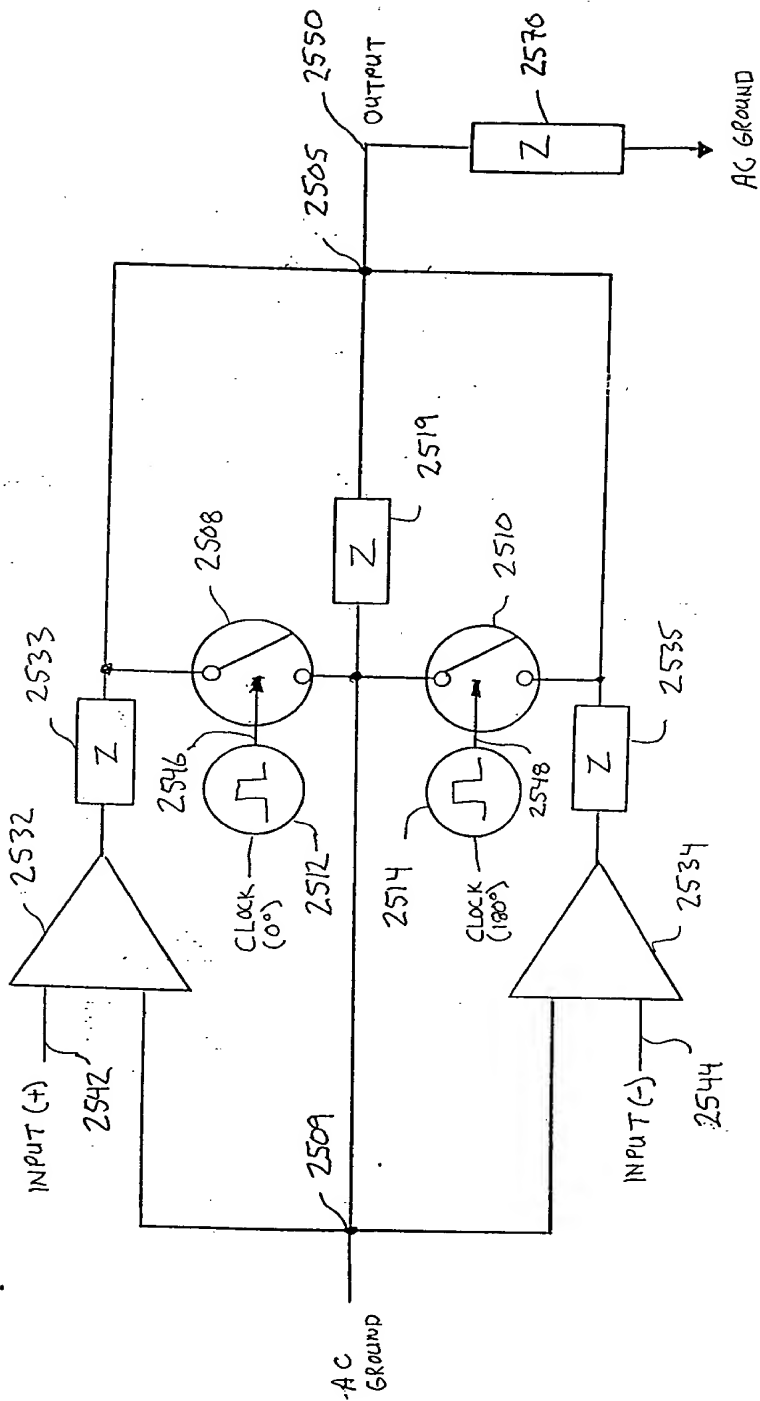


FIG. 25A

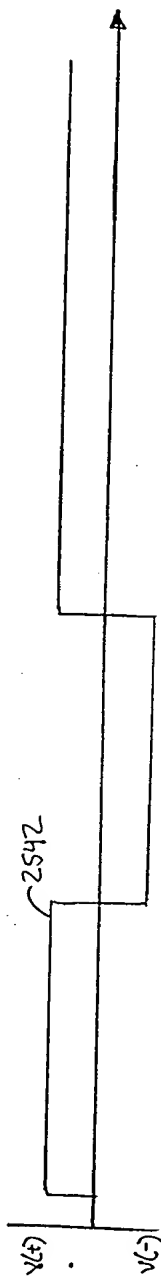


FIG. 25B

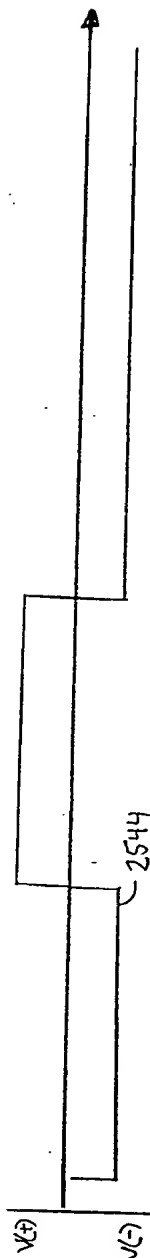


FIG. 25C

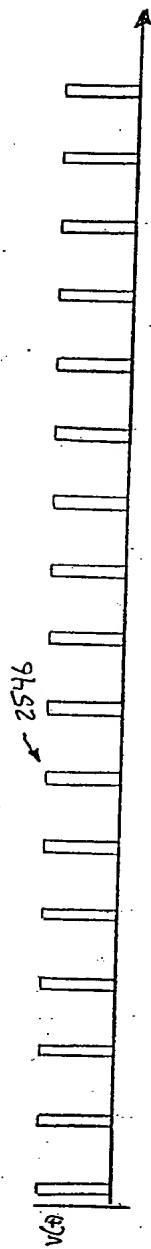


FIG. 25D

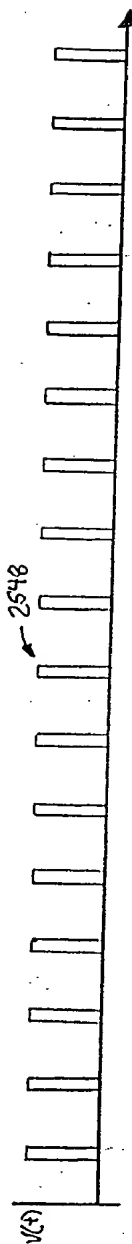


FIG. 25E

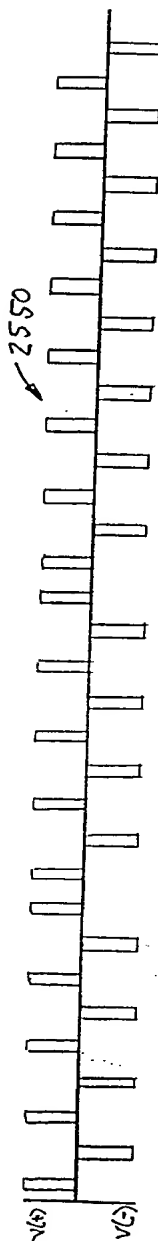


FIG. 25F

2602

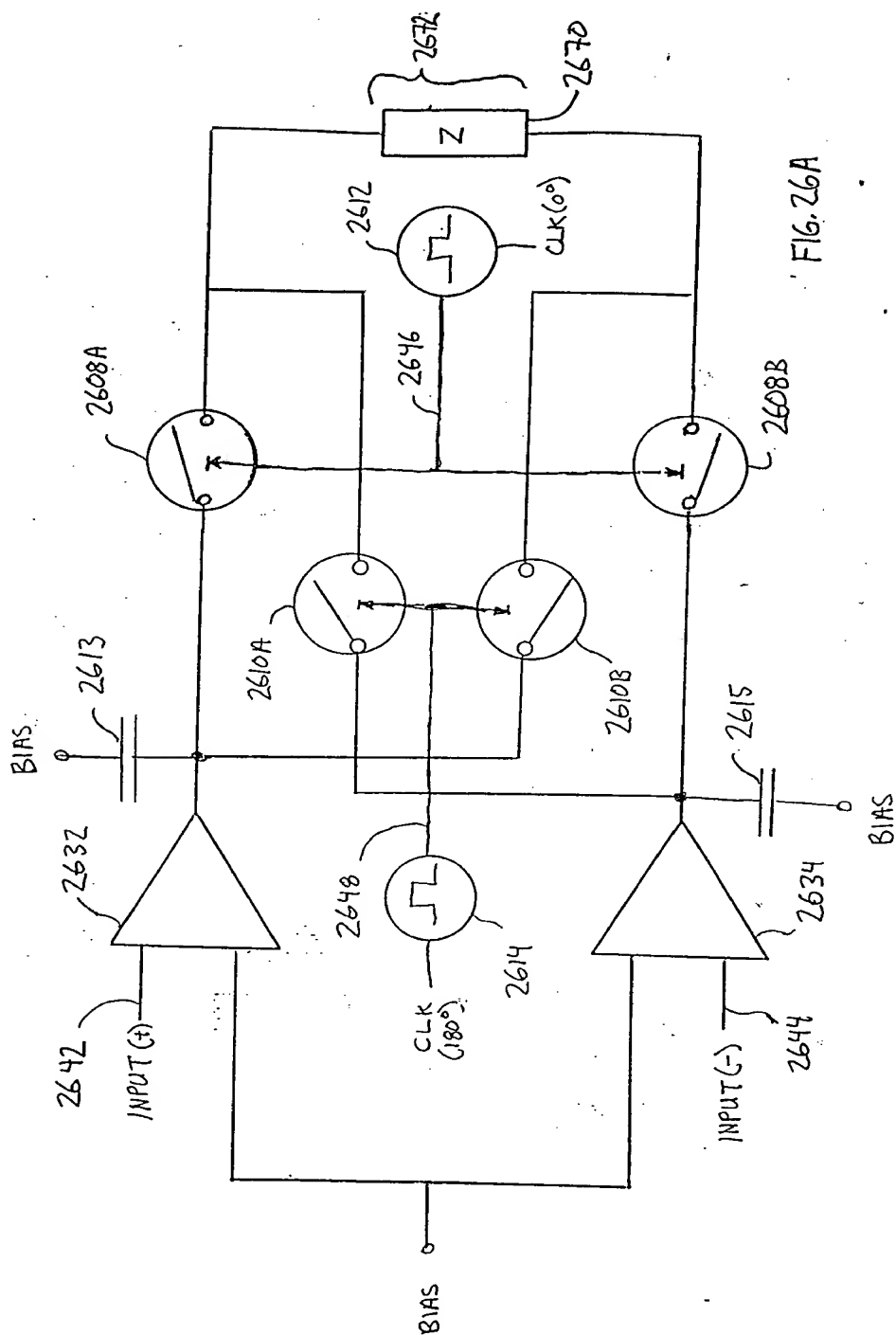


FIG. 26A

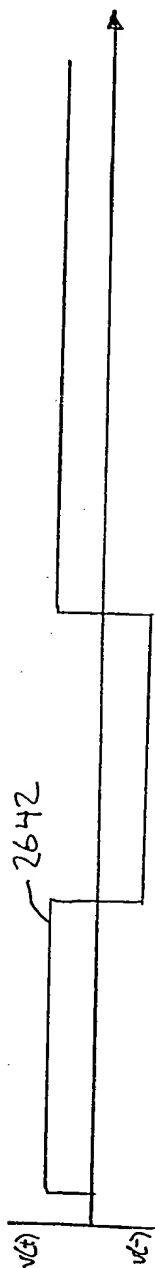


FIG. 26B

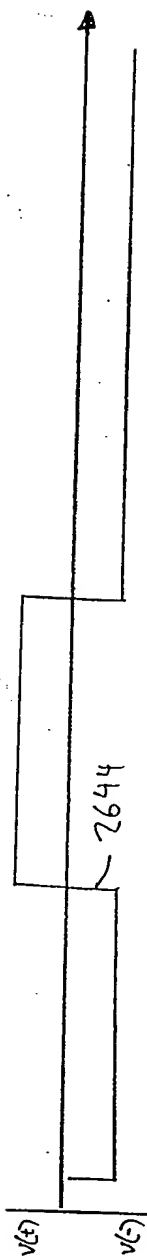


FIG. 26C

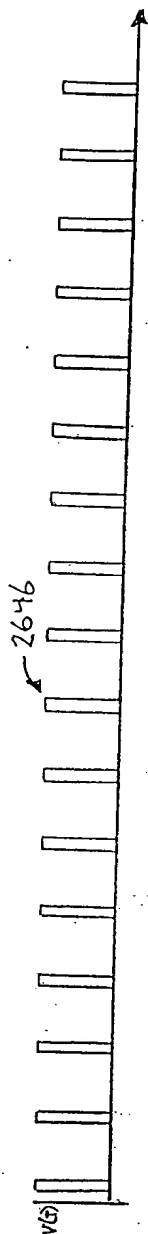


FIG. 26D

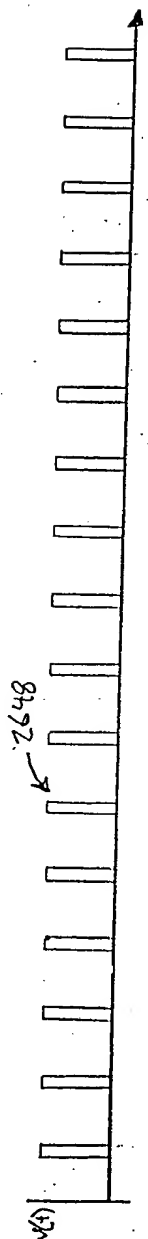


FIG. 26E

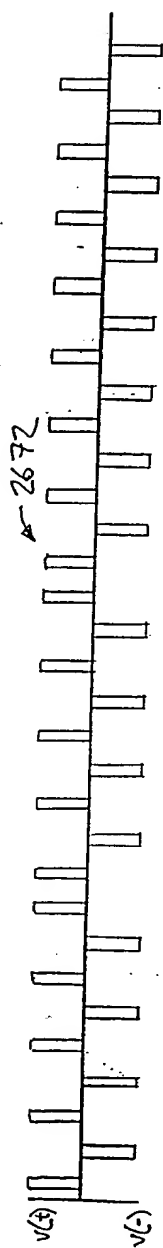


FIG. 26F

2702

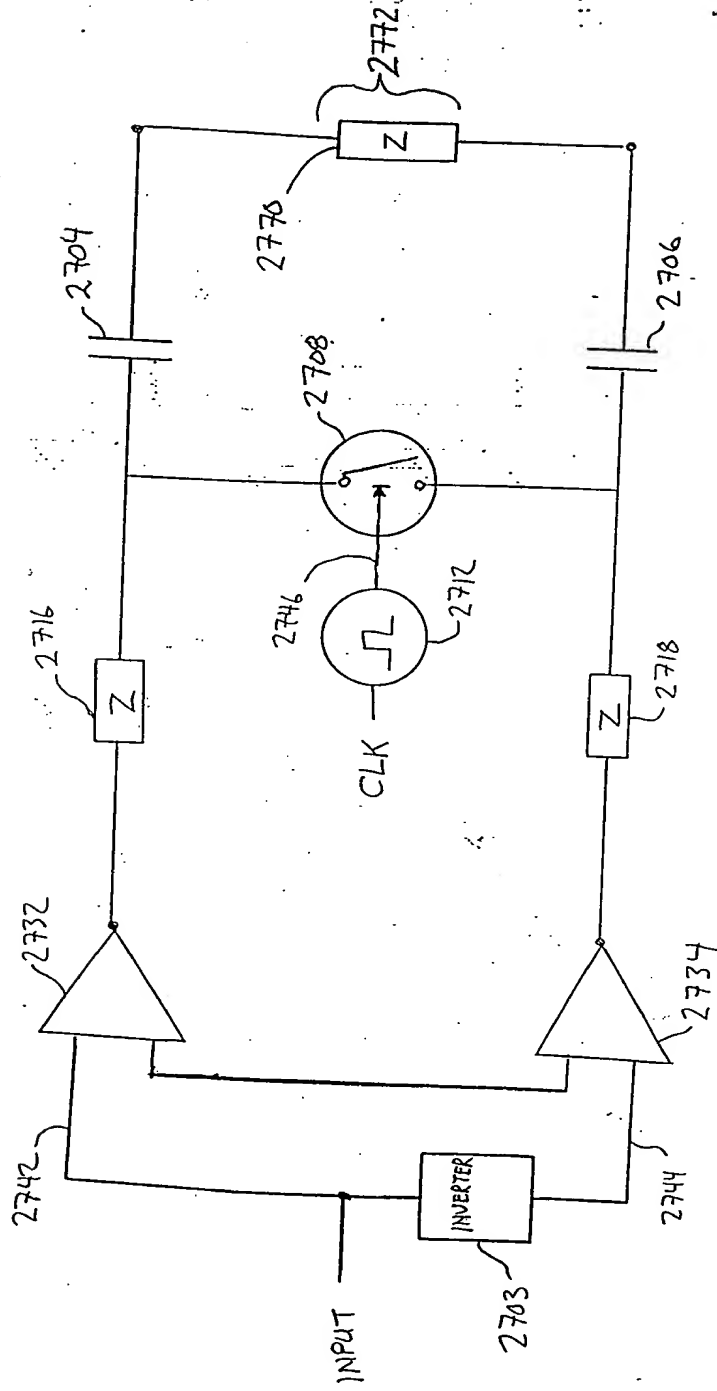
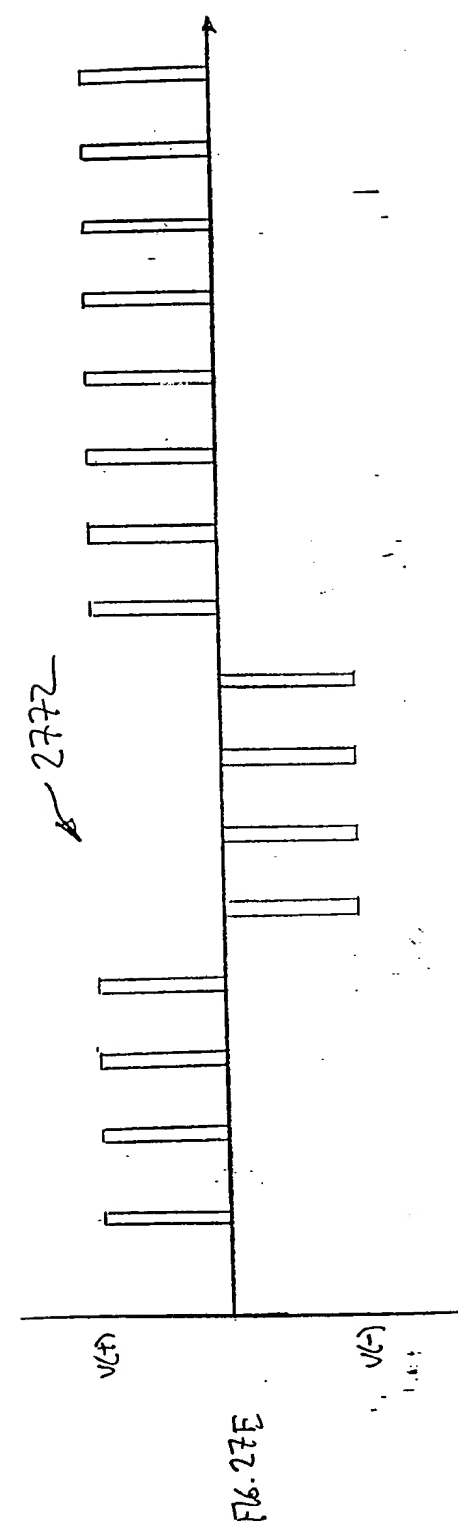
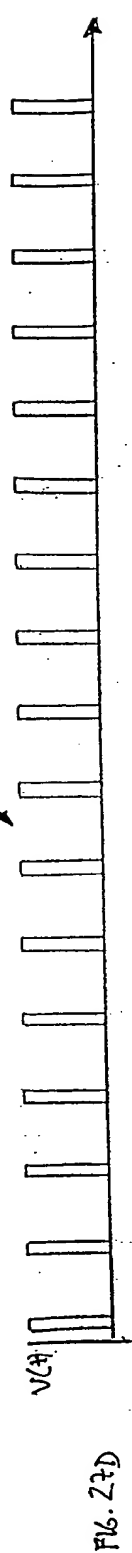
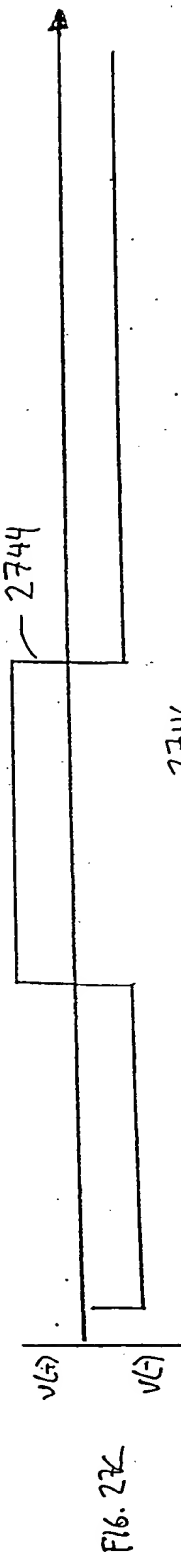
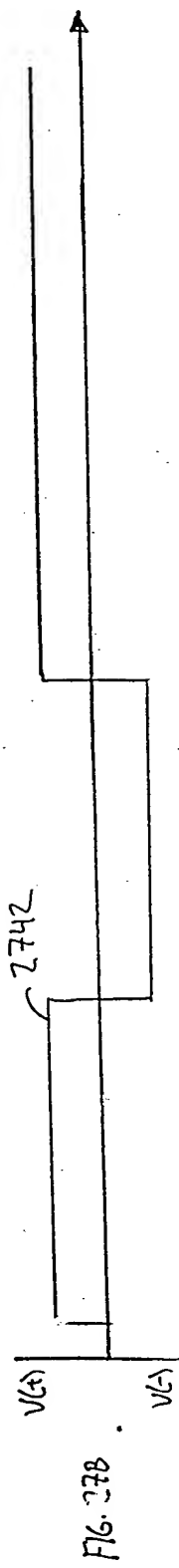


FIG. 27A





2800

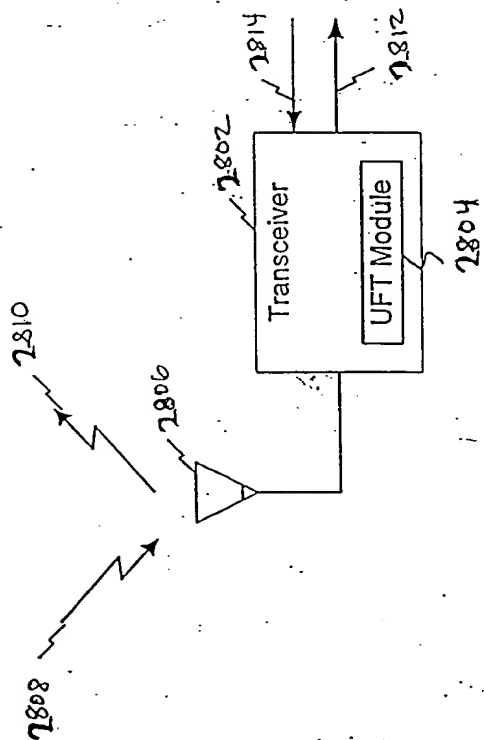
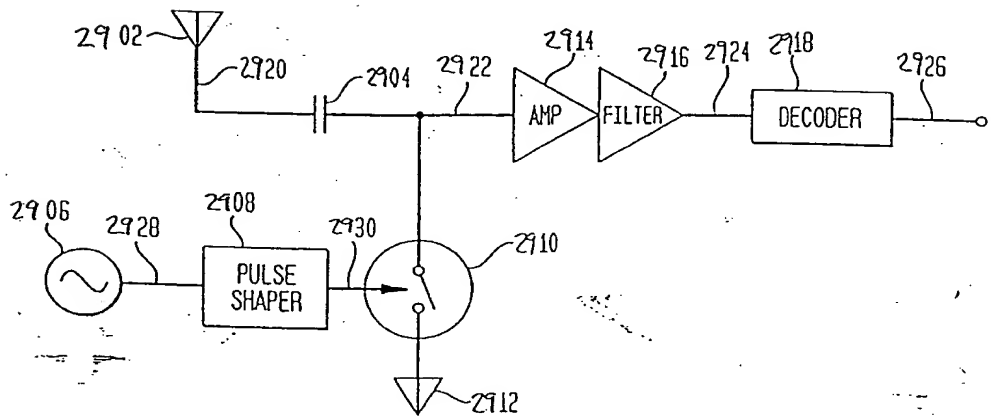


FIG. 28

FIG. 29  
 EXEMPLARY RECEIVER FOR  
 UNIVERSAL FREQUENCY DOWN-CONVERSION



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09855851.051604

FIG. 30

EXEMPLARY TRANSMITTER USING  
THE PRESENT INVENTION

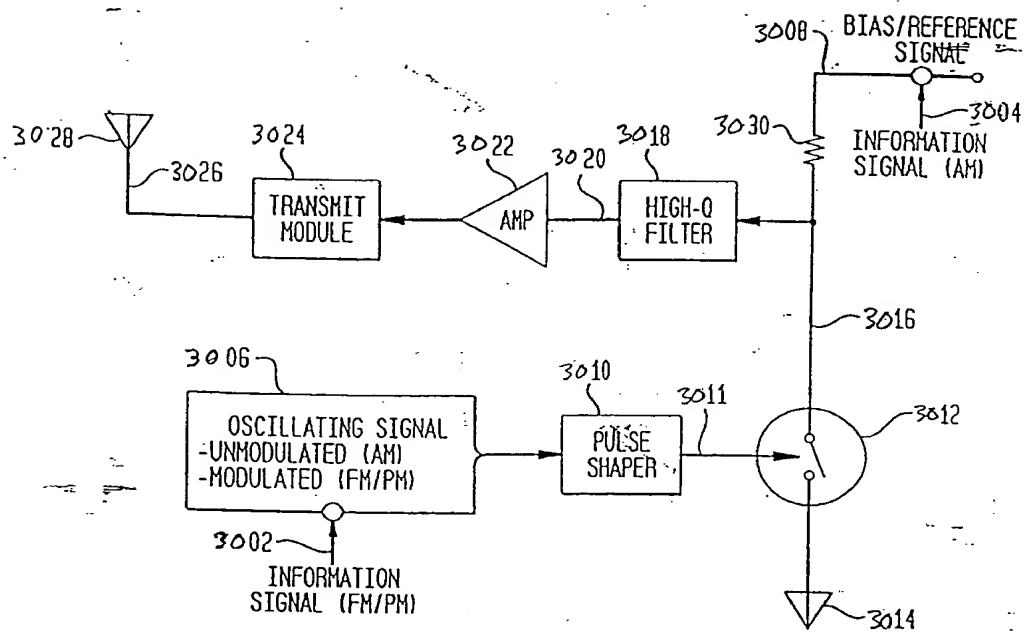
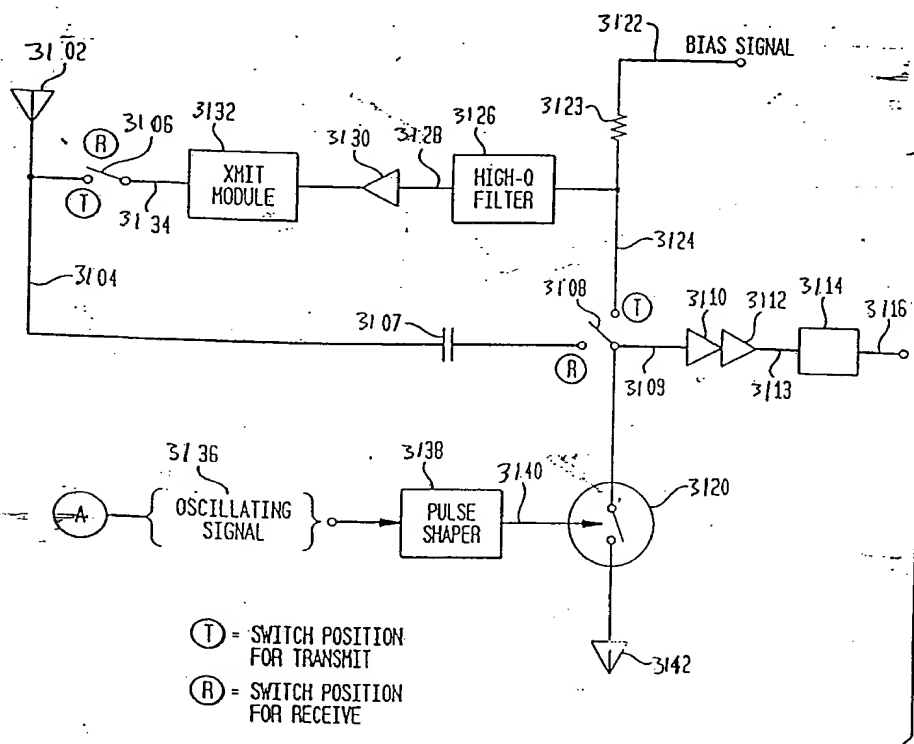


FIG. 31A

TRANSMITTER USING PRESENT INVENTION IN A  
HALF DUPLEX COMMUNICATIONS CIRCUIT WITH A  
UNIVERSAL FREQUENCY DOWN-CONVERTER (FM & PM)



09855851.051601

FIG. 31B

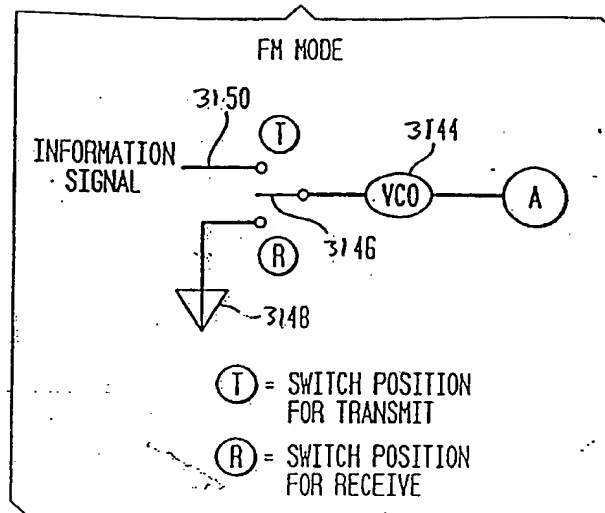


FIG. 31C

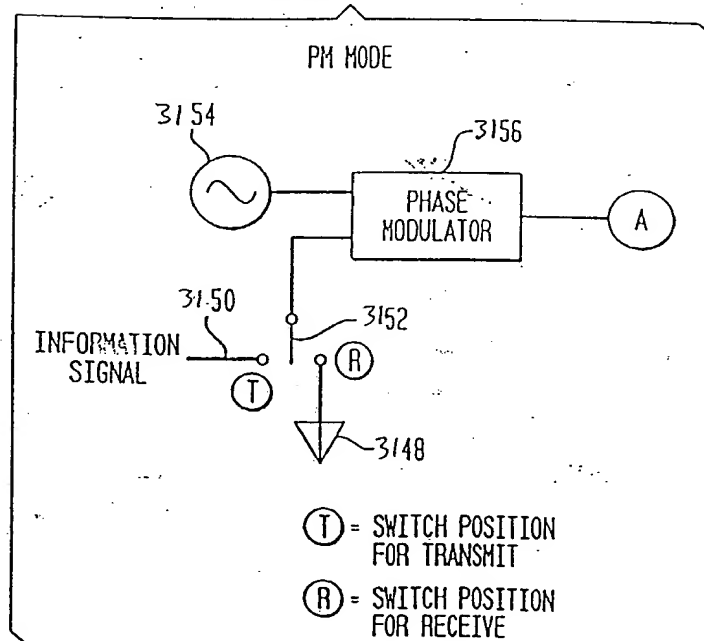
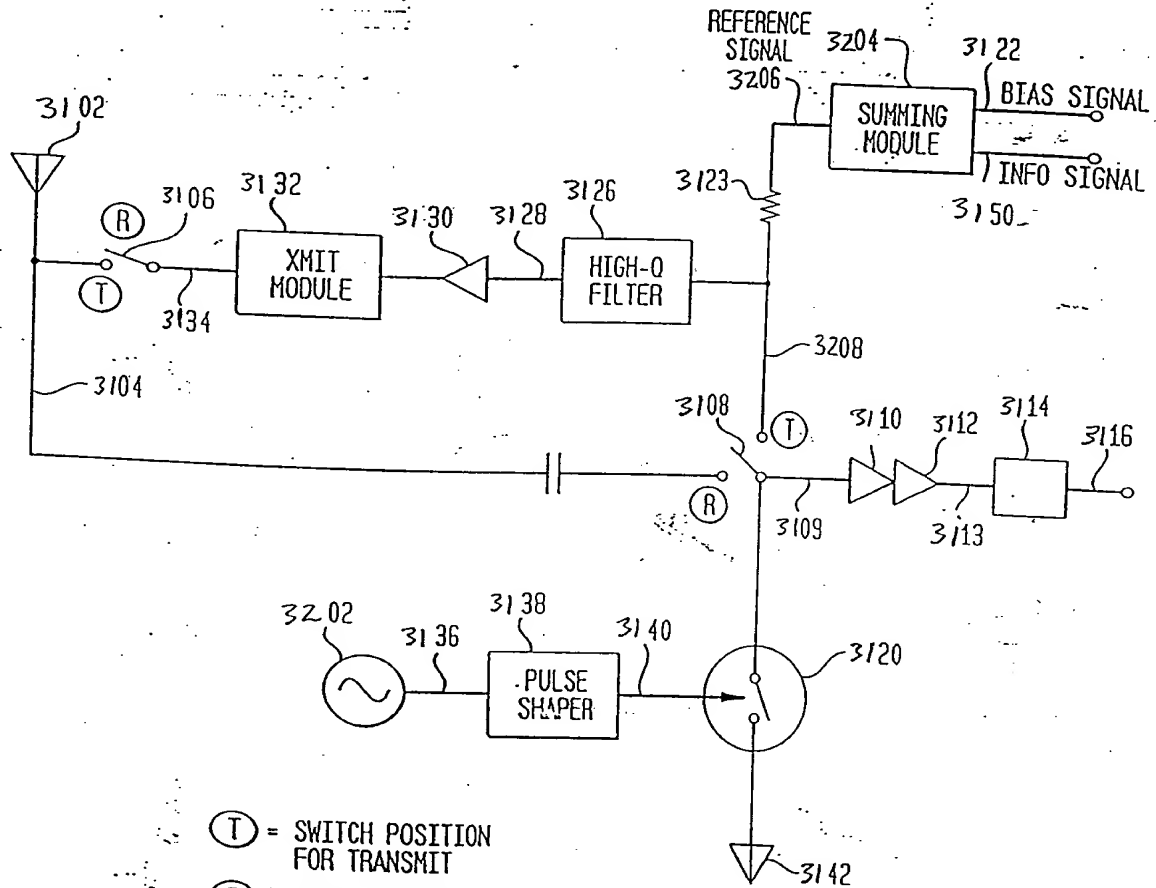


FIG. 32

TRANSMITTER USING PRESENT INVENTION IN  
A HALF-DUPLEX COMMUNICATIONS CIRCUIT  
WITH A UNIVERSAL FREQUENCY DOWN-CONVERTER (AM)



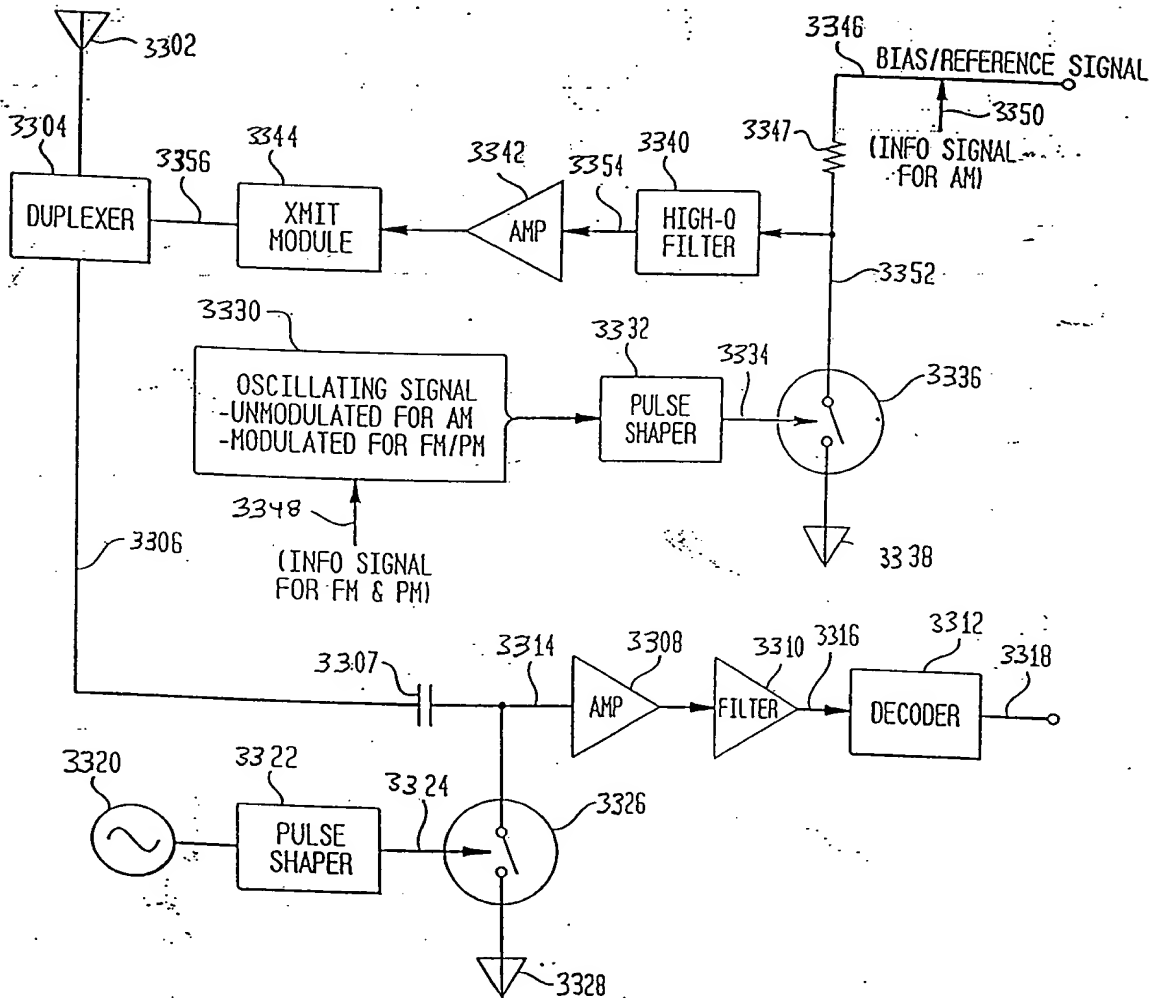
(T) = SWITCH POSITION  
FOR TRANSMIT  
(R) = SWITCH POSITION  
FOR RECEIVE

09855854 054604

095554 051604  
T09T50" T855960

FIG. 33

TRANSMITTER USING PRESENT INVENTION IN  
FULL DUPLEX COMMUNICATIONS CIRCUIT WITH  
UNIVERSAL FREQUENCY DOWN-CONVERTER





3402

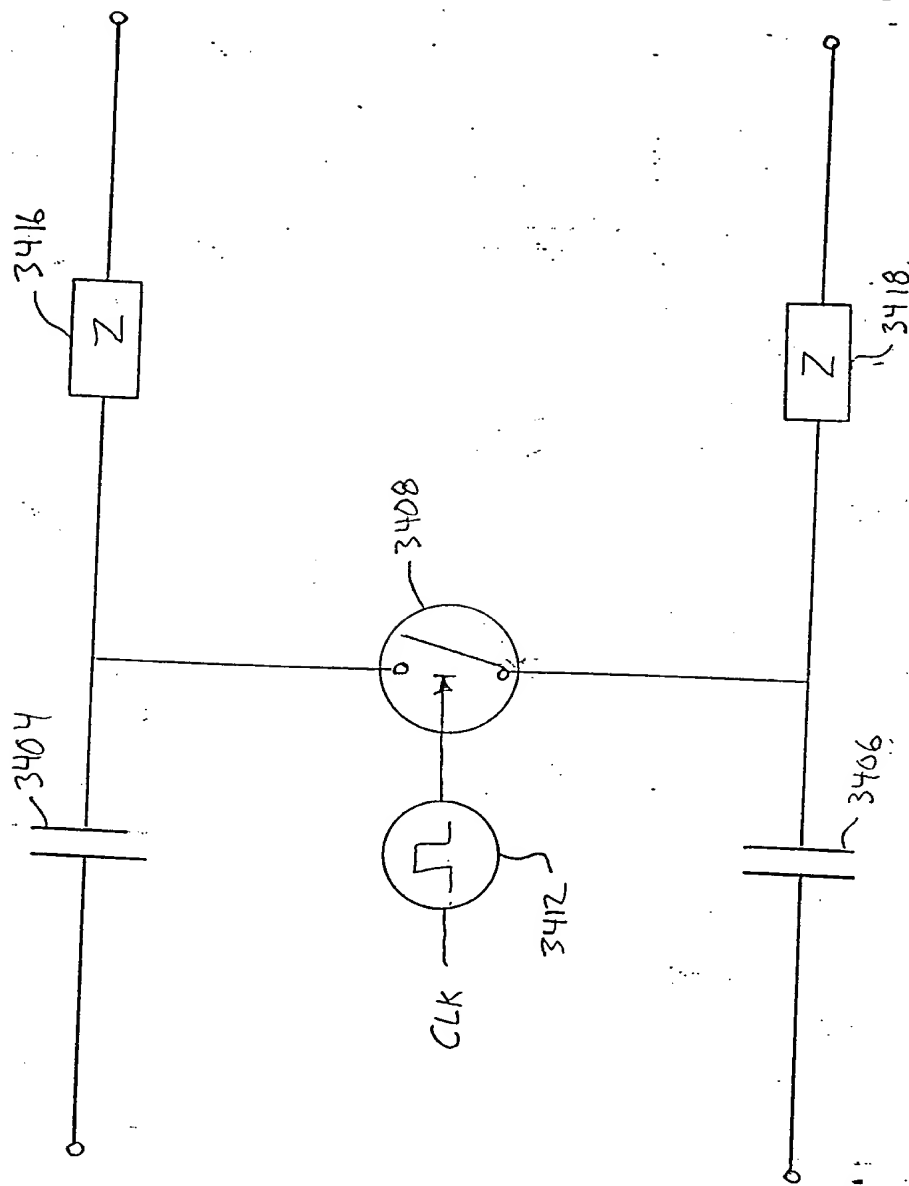


FIG. 34

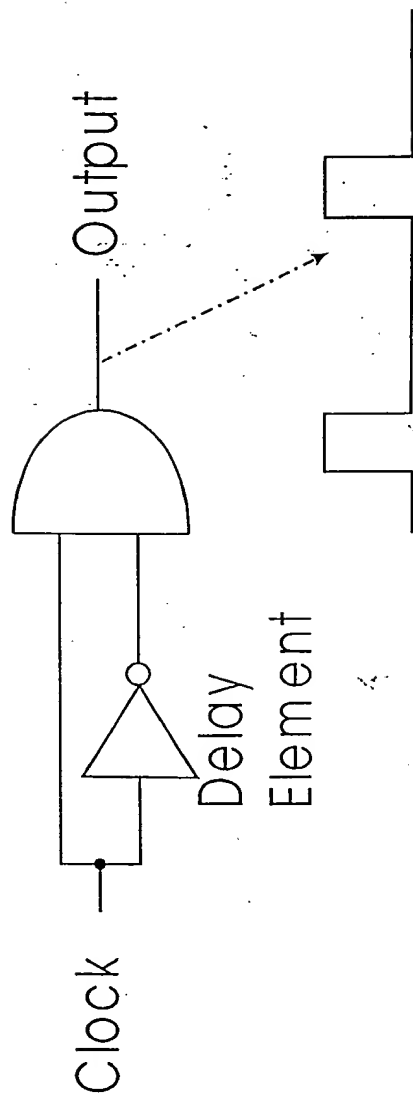


FIG. 35

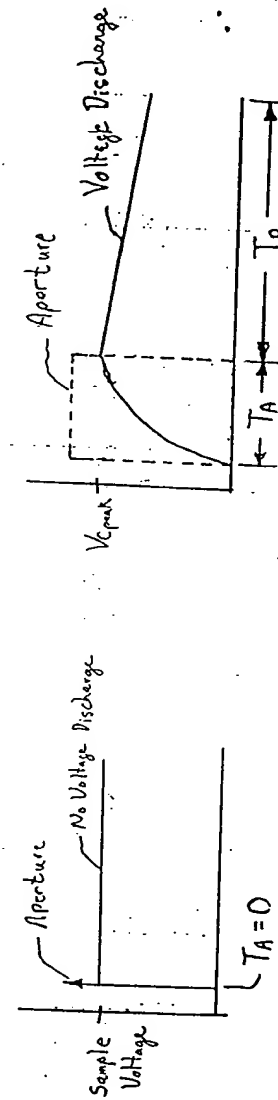
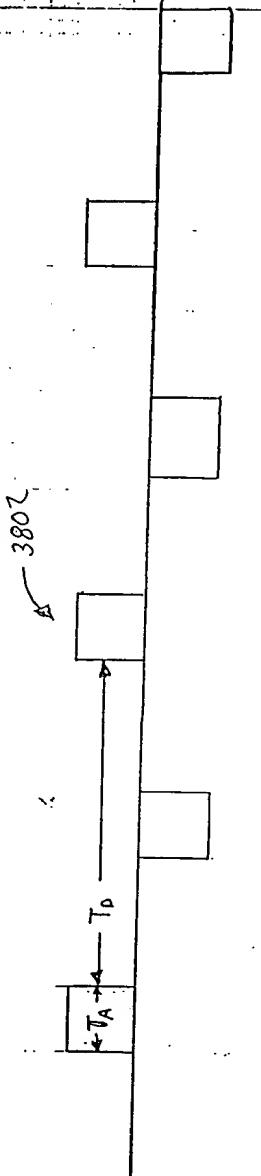
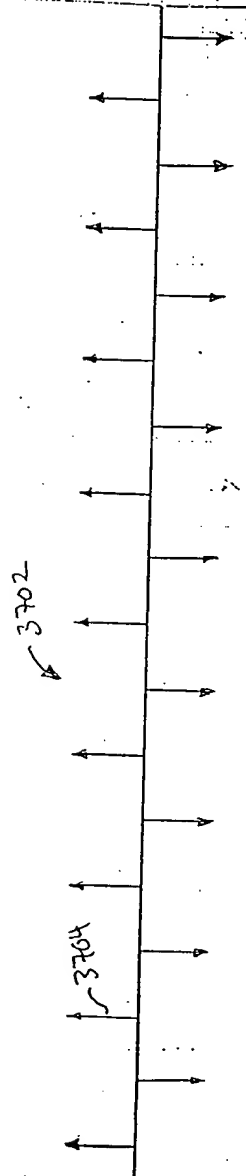
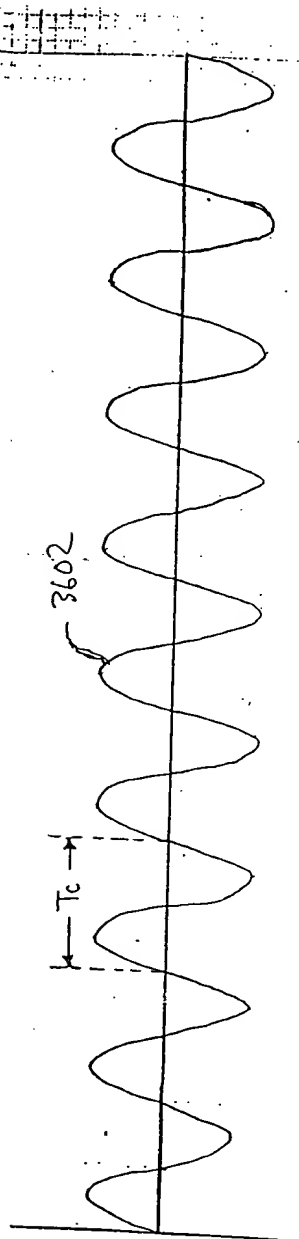


FIG. 40

FIG. 39

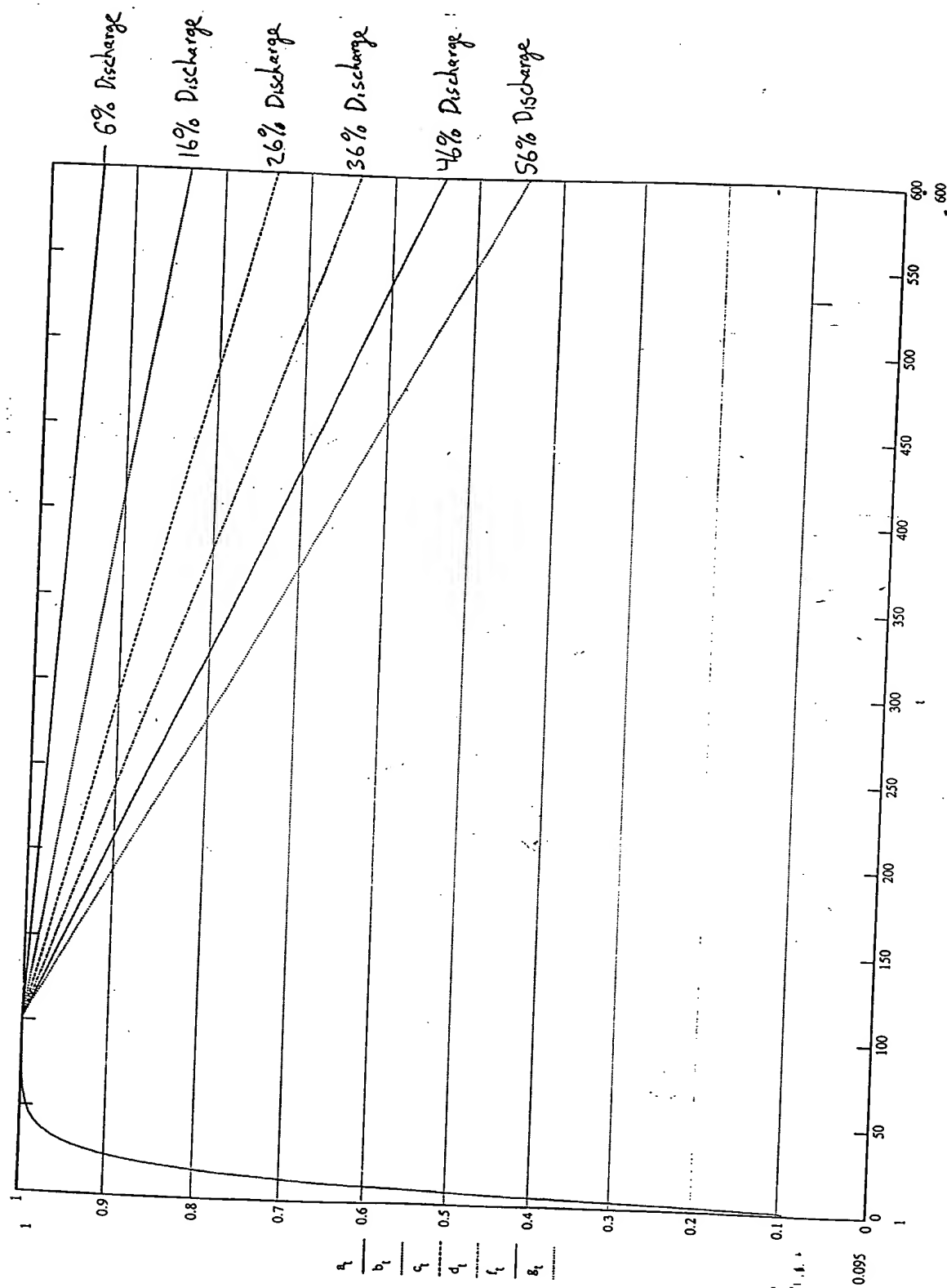


FIG. 41

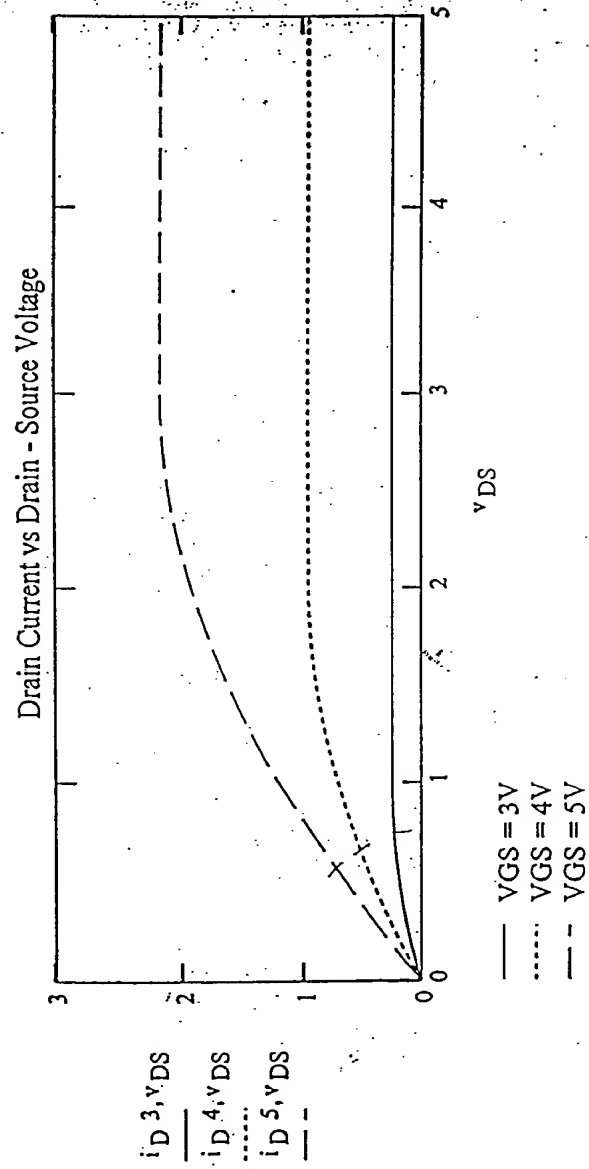


FIG 42

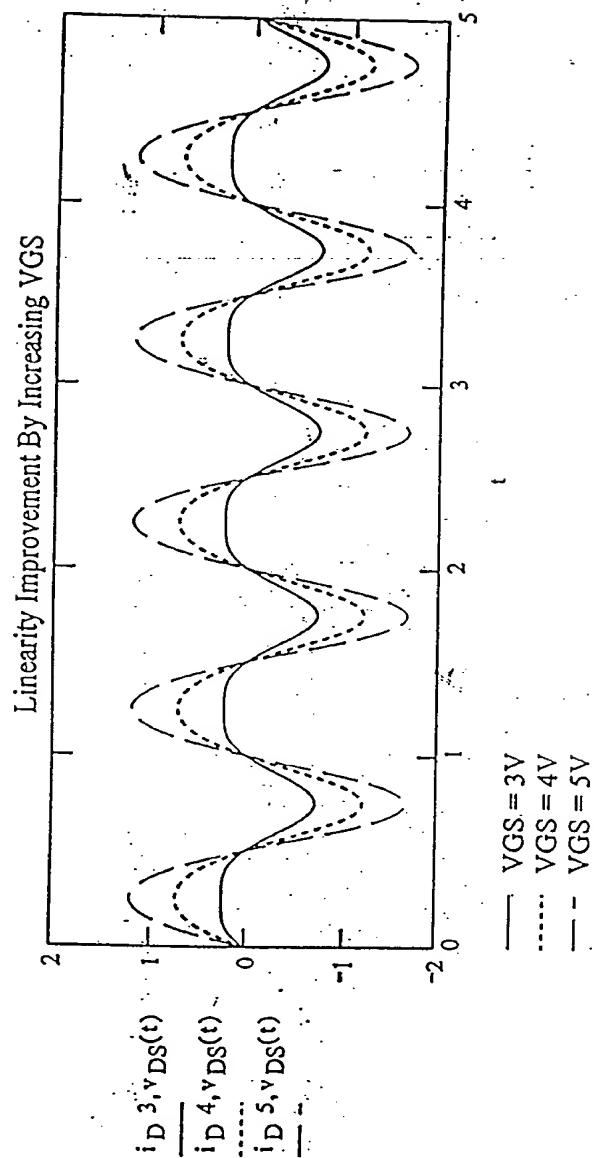
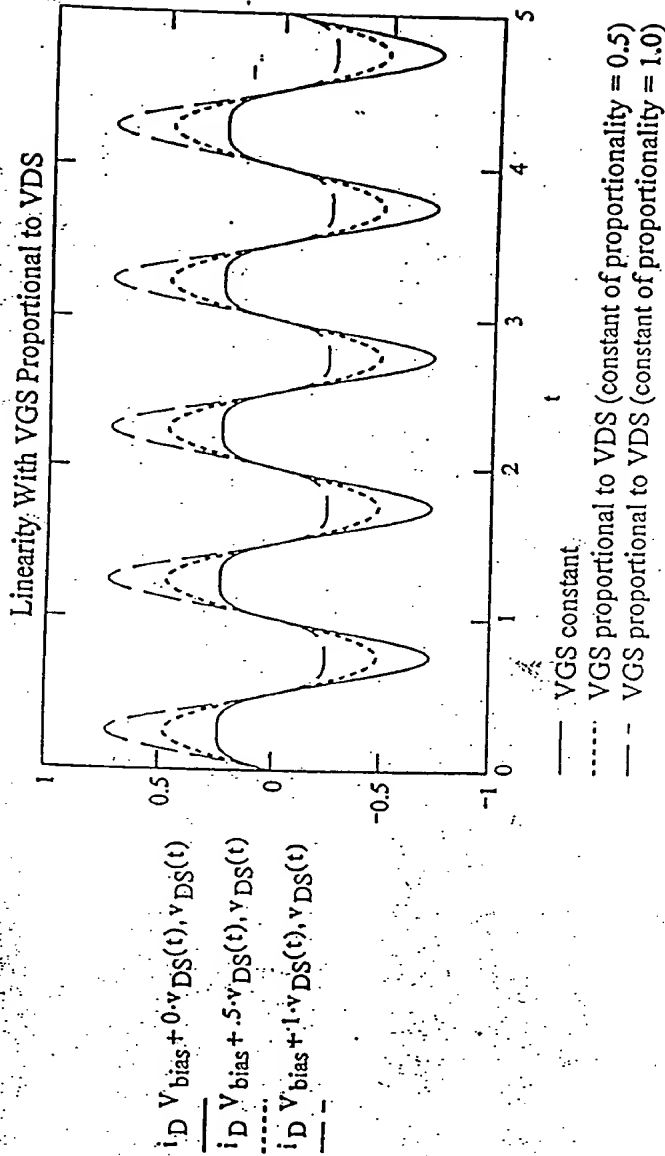


FIG. 43



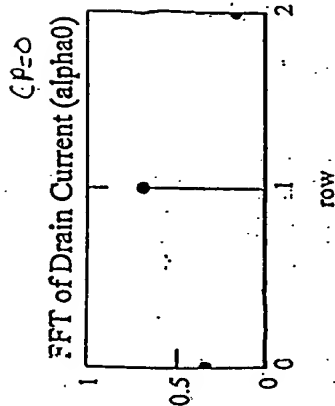


FIG. 45A

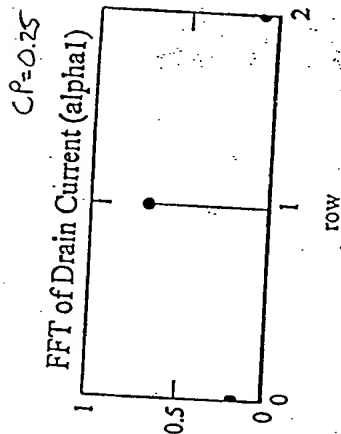


FIG. 45B

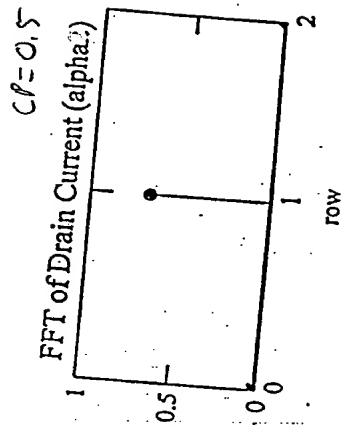


FIG. 45C

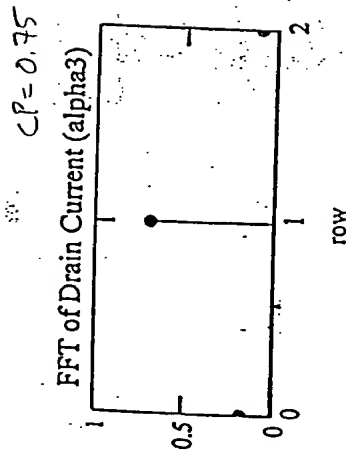


FIG. 45D

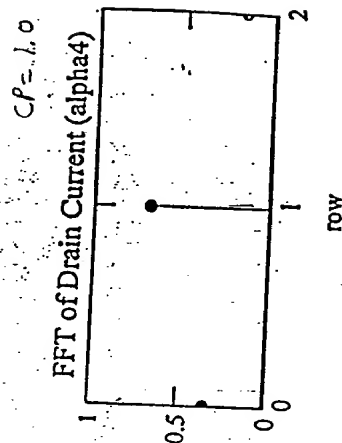


FIG. 45E



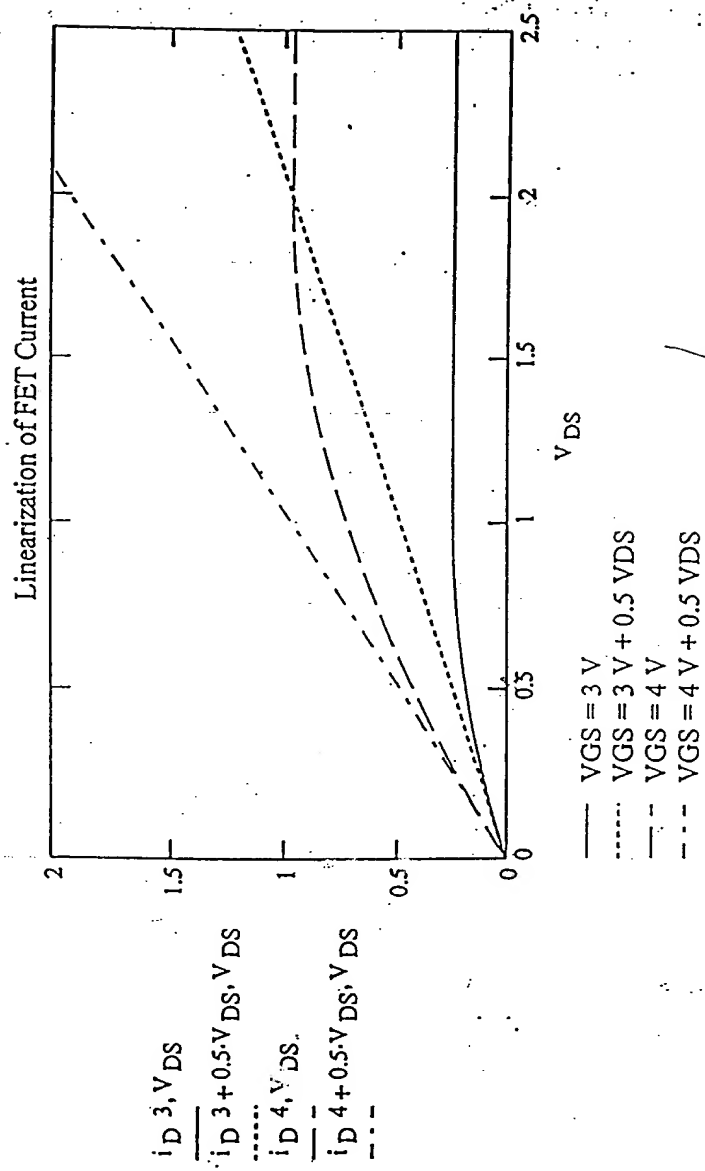


Fig. 46

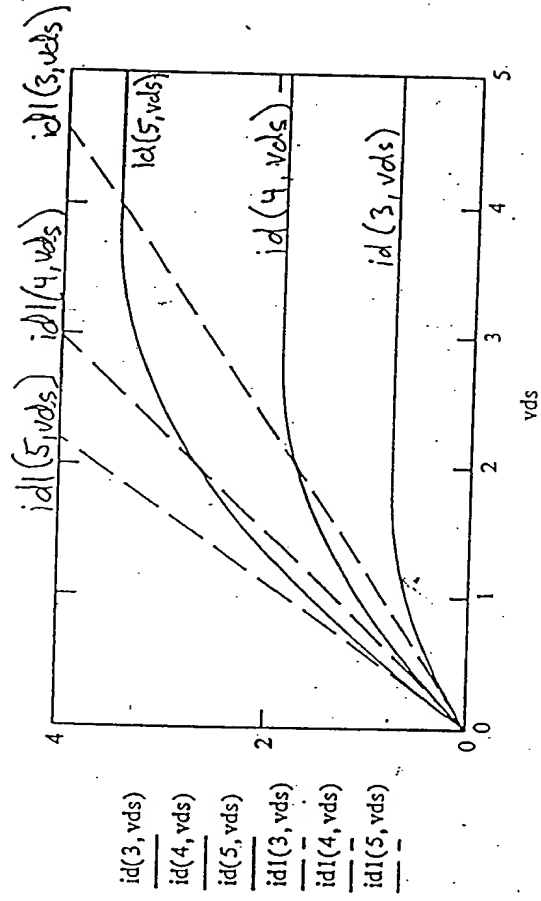
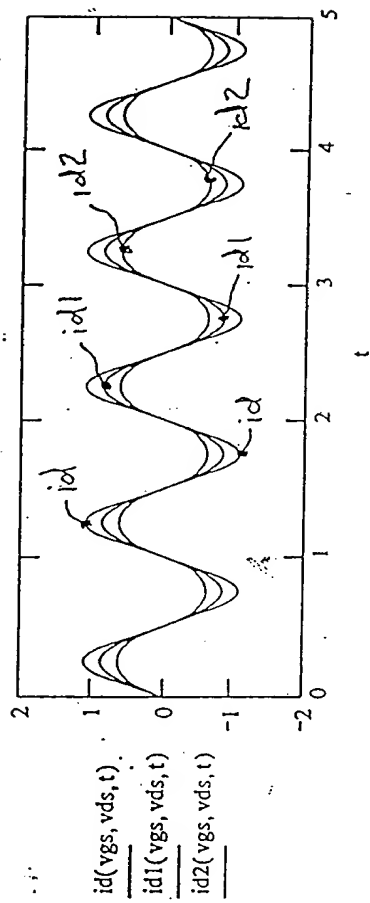


FIG. 47



F16, 48

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T09T50 T585860

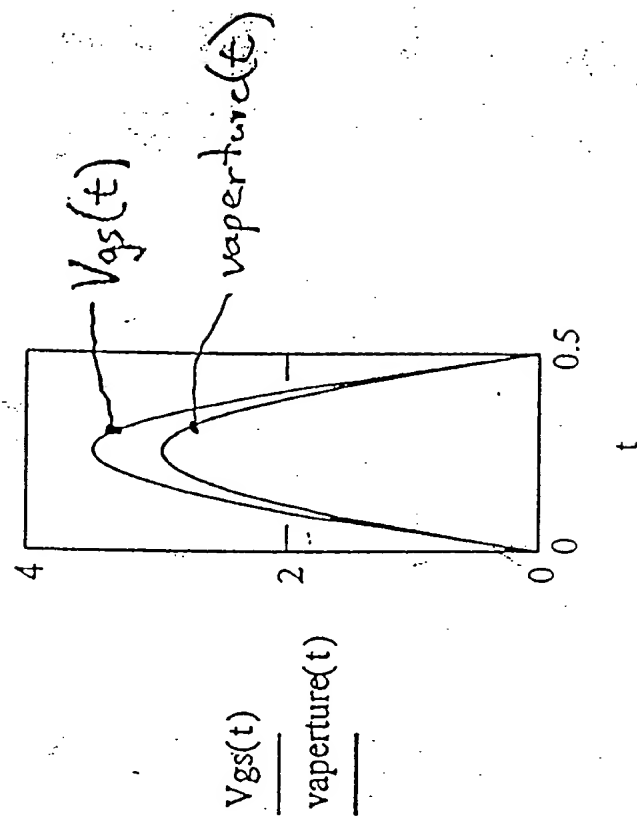


FIG. 49

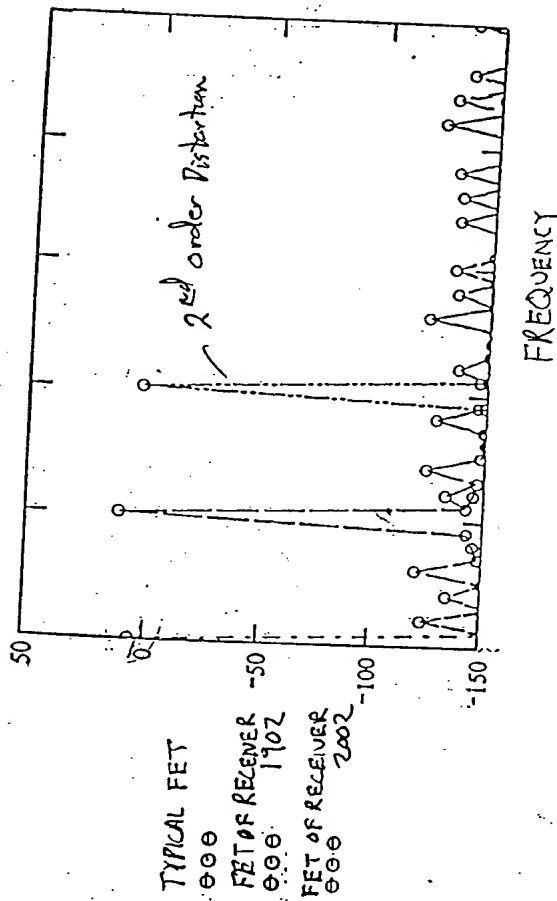


FIG. 50

FOOTNOTES

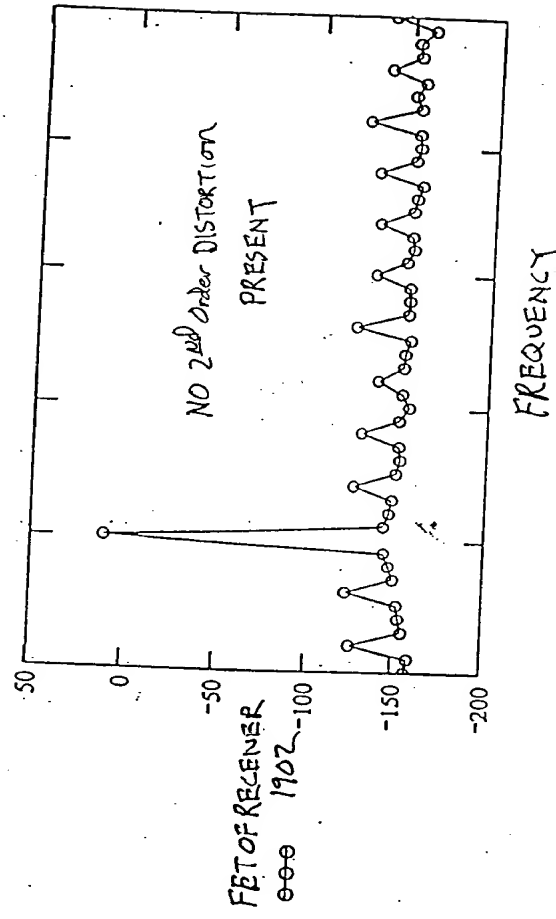


FIG. 51

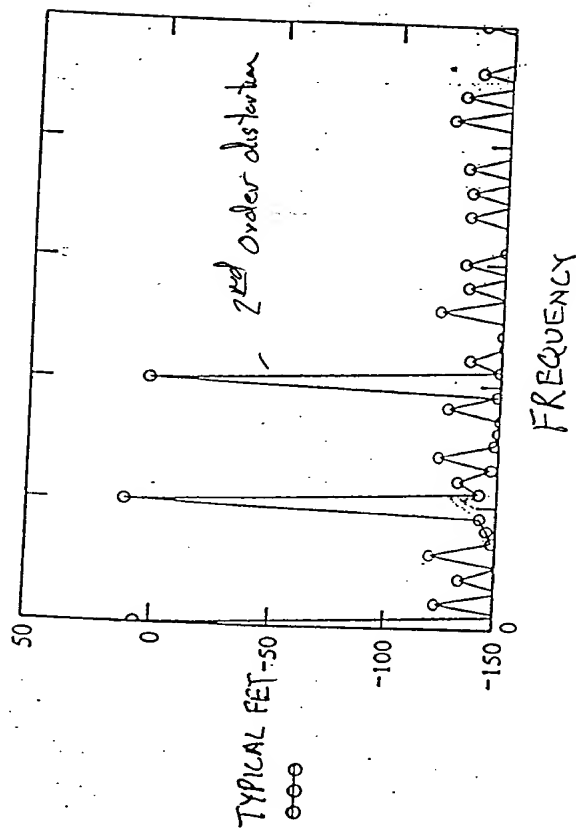


FIG. 52

095554 051601

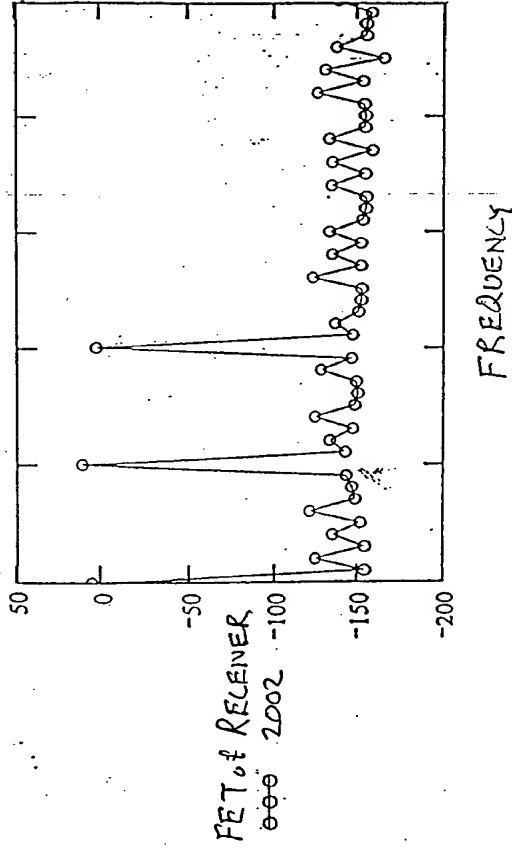


FIG. 53



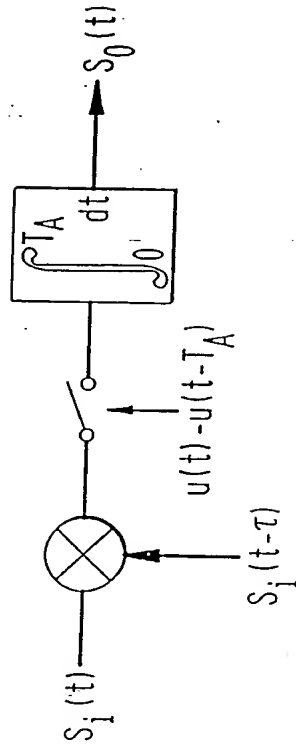


FIG. 54

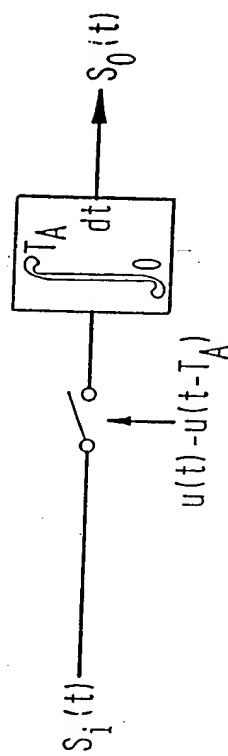


FIG. 55

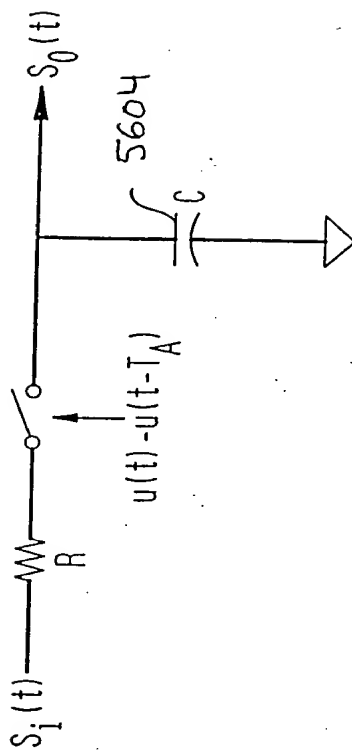


FIG. 56

# UFT OUTPUT CHARGE TRANSFER

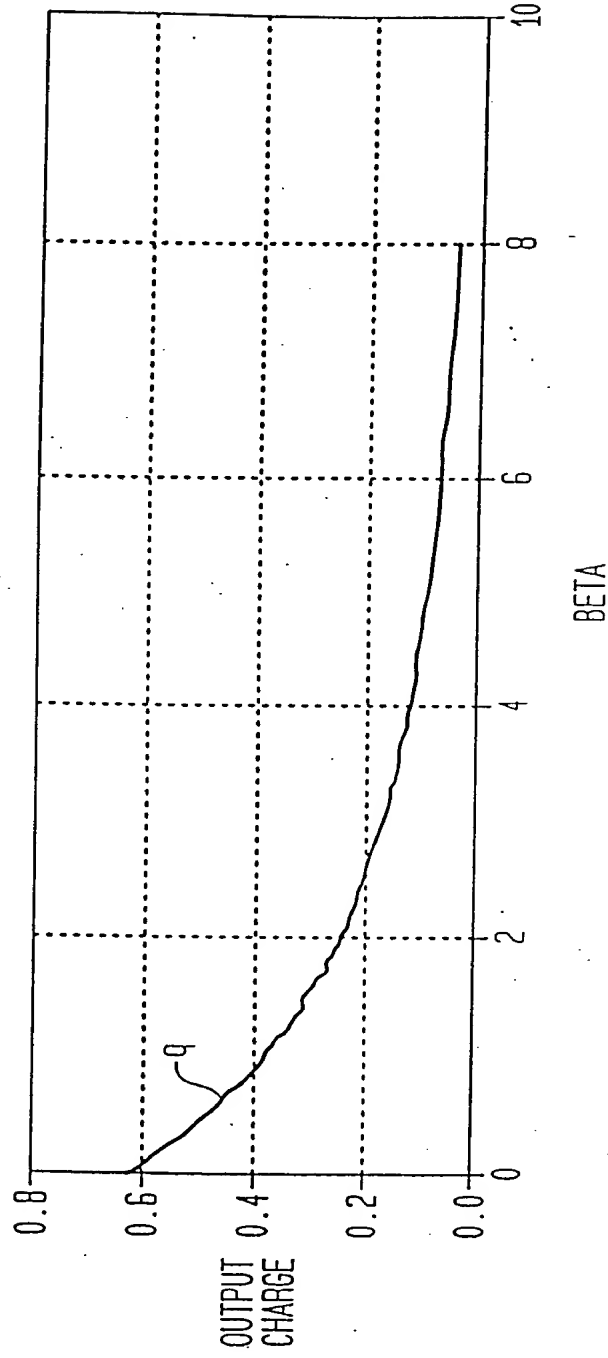


FIG. 57

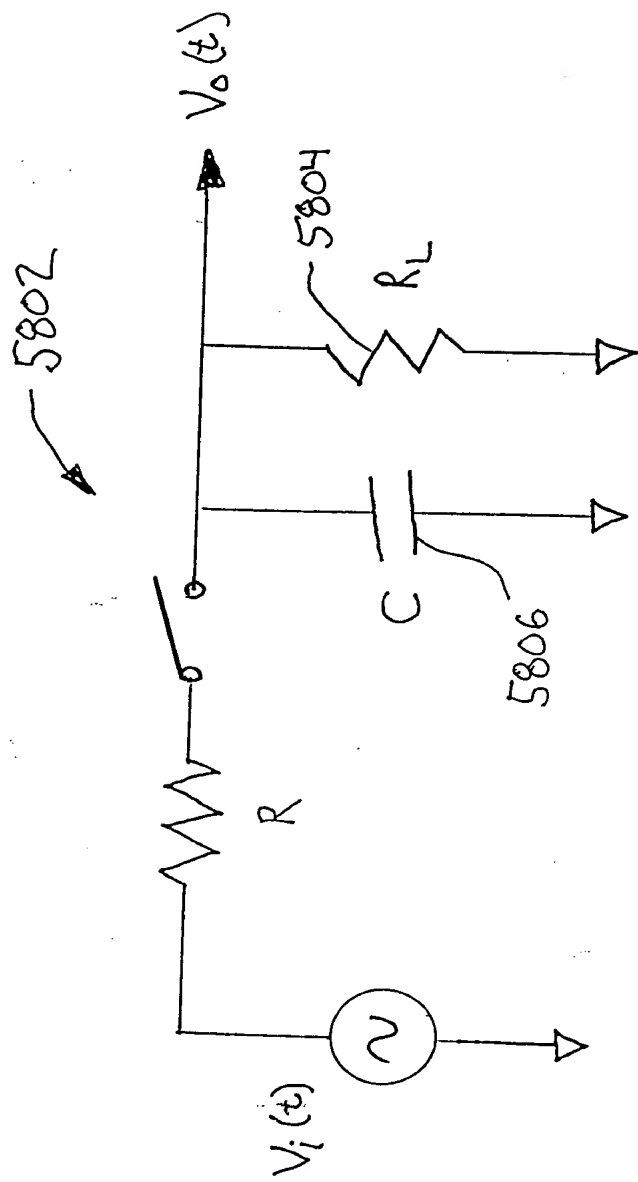


FIG. 58

TOP SECRET 50-105404

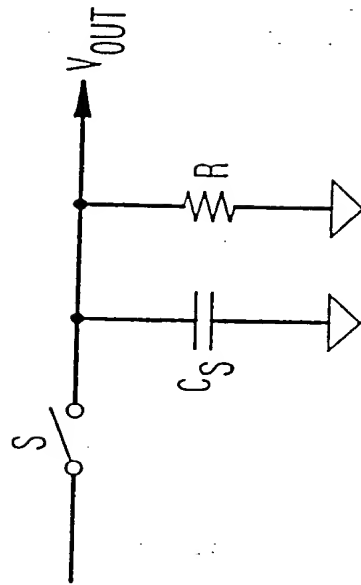


FIG. 59

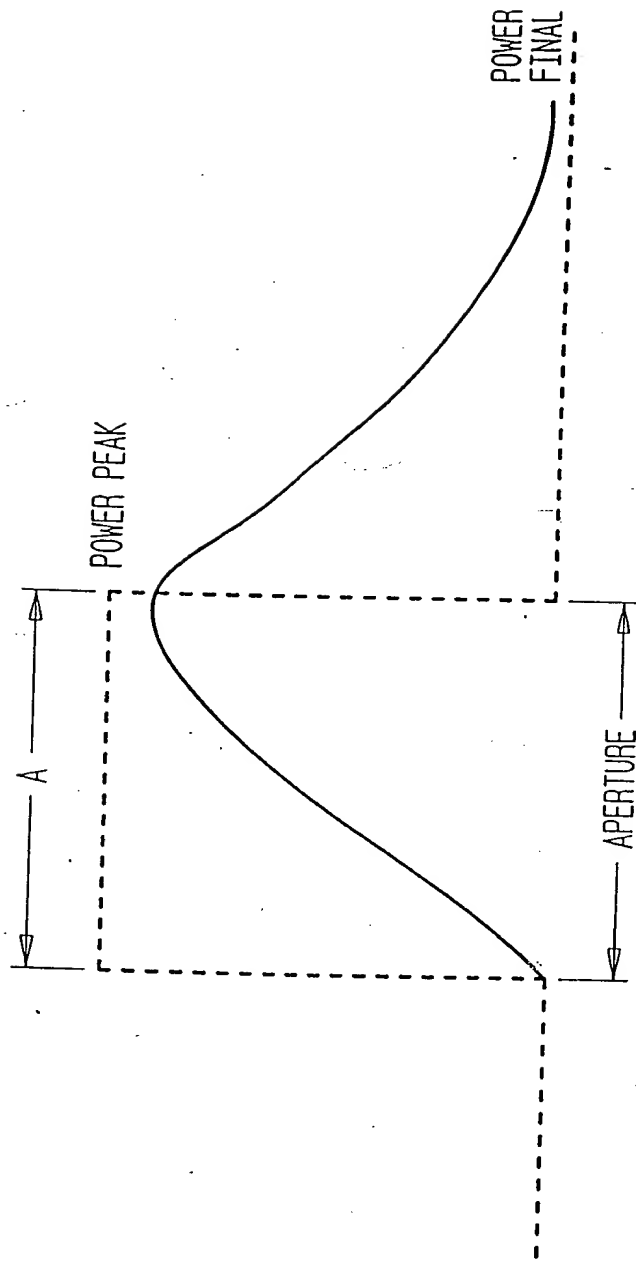


FIG. 60

09855854 051604

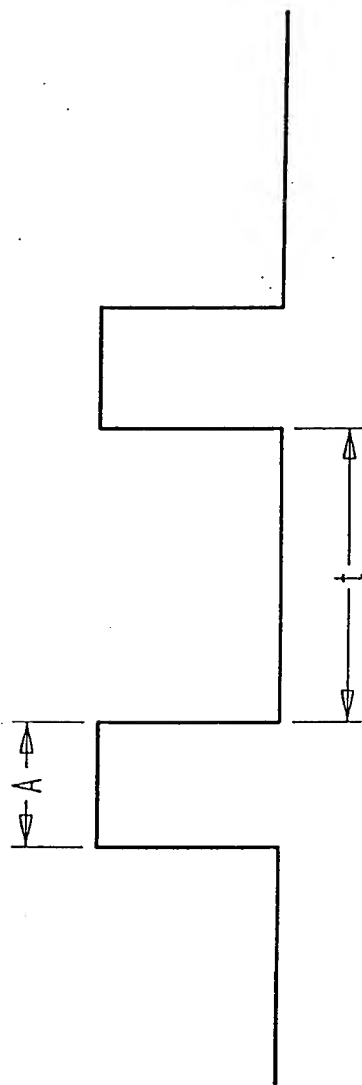


FIG. 61



METHOD FOR DOWN-CONVERTING AN ELECTROMAGNETIC  
SIGNAL

6200

RECEIVE A RF INFORMATION SIGNAL

~6202

ELECTRICALLY COUPLE THE RF INFORMATION SIGNAL TO A  
CAPACITOR

~6204

CONTROL A CHARGING AND DISCHARGING CYCLE OF THE  
CAPACITOR WITH A SWITCHING DEVICE ELECTRICALLY  
COUPLED TO THE CAPACITOR

~6206

PERFORM A PLURALITY OF CHARGING AND DISCHARGING  
CYCLES OF THE CAPACITOR, THEREBY FORMING A DOWN-  
CONVERTED INFORMATION SIGNAL

~6208

END

~6210

FIG 62

09855851, 051601